Ka-band MEMS SPDT Switch GaAs MMIC

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Abstract
A wideband (25-35GHz) Ka-band SPDT switch using MEMS on GaAs MMIC process is designed, fabricated and tested on-wafer. The switch exhibits a measured insertion loss of 0.9±0.1dB, over the band, with isolation of 18dB minimum. The return loss at ports is more than 17 dB. The switch is controlled using two terminals connected to actuating pad of each MEMS switch. The advantage of MEMS on GaAs MMIC process is on-chip integration with high performance GaAs MMICs. The switch is designed and simulated using 2.5D and 3D field solvers and simulated & measured results are presented and compared. This switch consumes negligible power.

Keywords: MEMS, MMIC, SPDT, Switch, Ka-Band, GaAs, SoC, High linearity.

I. Introduction

Microwave switches play a vital role in a radar technology as well as in communication systems. They are used in a variety of applications, such as in satellite payload for selection between main and redundant sub-systems, in digital attenuator and phase shifters for selecting reference & attenuating/phase-shifting paths, and in transmit-receive modules with common antenna. Microwave switches can be implemented using FET, PIN diode, waveguides, etc [1]. Lately, MEMS based switches have exhibited very low insertion loss & excellent isolation in microwave frequencies with very small foot print in line with FET and PIN diode switches. Like solid state switches, MEMS based switches can easily be integrated with GaAs or Si based high performance MMICs [2].

Keeping in view the demands of the application, one of the above elements can be used to construct an SPDT switch. For satellite based subsystems where, along with performance, space, mass & power budget is of prime concern, solid state switches are used. Complex biasing network requirements of PIN diode switches & high insertion loss of FET based switches [1] at high frequencies like Ka-band & beyond, give enough impetus to explore the possibility of MEMS based switches [3].

In this paper, MEMS on GaAs MMIC process has been used to demonstrate a low loss solution to redundant dual LNA application at Ka-band. The same MMIC process is also used to develop the Ka-band dual LNAs. This ensures that in next step, the MEMS switch can be integrated with dual LNA to give a bond-wire free single chip configuration with redundancy at Ka-band.

The front-end of Ka-band payload consists of a 2:1 redundant Ka-band LNA MMIC along with an SPDT switch, as shown in Fig. 1. These two LNAs are designed using GaAs/InAlAs based 0.13 um MHEMT MMIC process, and are fabricated on a single chip. This MMIC has two RF inputs and two outputs.

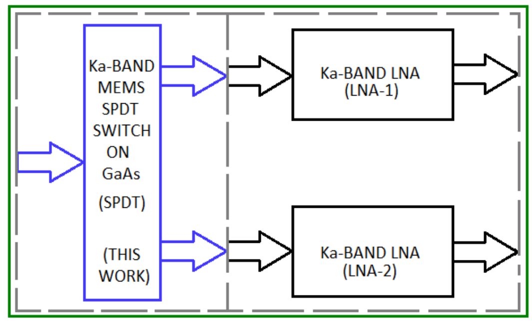


Fig. 1. Block diagram of Ka-band dual LNA with input MEMS SPDT switch on GaAs

The input of Ka-band dual LNA has a low loss SPDT switch & output is combined with a hybrid. For achieving a compact, reliable and parasitic free (as described earlier) solution, the Ka-band MEMS SPDT switch is fabricated on the same GaAs substrate. The details of design are presented in next section and the performance is discussed in section-III.

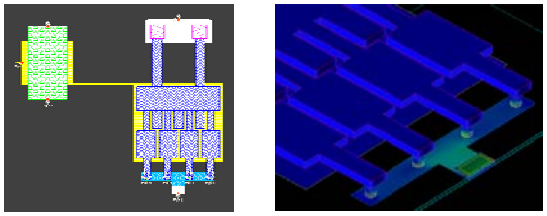
II. Design Methodology

The target specifications of the Ka-band SPDT Switch are as below:

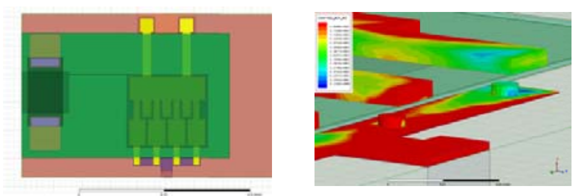
TABLE I
MAJOR SPECIFICATIONS

Parameters	Unit	Specifications
RF Frequency Band	GHz	25 – 35
Insertion Loss, Max.	dB	1.0
Isolation, Min.	dB	18
Insertion Loss Variation	dB	± 0.1
Input/Output Ports Impedance	Ohms	50
Return Loss at I/O Ports, Min.	dB	18
Actuation Voltage	V	70 ±2

MEMS cell EM model: A direct contact type MEMS cell is used as a basic switching element for designing the SPDT to meet the specifications in Table I. The MMIC process offers a SI GaAs/InAlAs substrate over which the MEMS cell is fabricated [4]. A designed cell layout is shown in Fig. 2. The cell is modeled with MEMS cantilever, pillar, contacts and actuation layer information along with existing MMIC layers and simulated with mesh frequency of 150 GHz, i.e, five times the frequency of operation. The same structure is modeled in 2.5D EM simulator as well as in a 3D solver. The simulation results for ON / OFF state of switch [5] using MoM technique (2.5D) as well as FEM (3D) is compared at 30 GHz, in Table II while details are given in Fig. 3 and Fig. 4.



(a) Layout (b) Post EM simulation view in 2.5D simulator



(c) 3D model (d) Post EM simulation view in OFF state in 3D simulator

Fig. 2. Modeling of MEMS series cell with decoupling resistor and capacitor in 2.5D and 3D EM solvers

The OFF state simulation in circuit simulator is taken from the 2.5D EM solution files, while for ON state, between each of the four contacts of MEMS cantilever & pillar, a 10 ohms resistor is added with EM solution, to take into account the contact resistance [6]. In 3D model, cantilever is pulled down to make a contact in ON state. These approximations may induce deviation with actual scenario and calls for mechanical modeling of MEMS switch in two states. This part is avoided here. Only electrical simulation is done in this work as MEMS cell is already designed structurally by foundry and optimized for best performance [4].

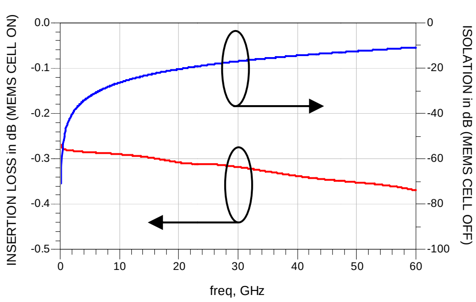


Fig. 3. EM simulation of MEMS Cell in ON and OFF state using MoM

Table II shows, both 2.5D and 3D simulation results are good enough to design the SPDT switch as still there is a good margin in single switch loss and target specification (<1dB) of insertion loss.

SPDT design: The MEMS based SPDT is required to feed into two inputs of dual LNA MMIC (Fig. 1) which is already designed and tested. The spacing between the two inputs of LNA is 1055 µm.

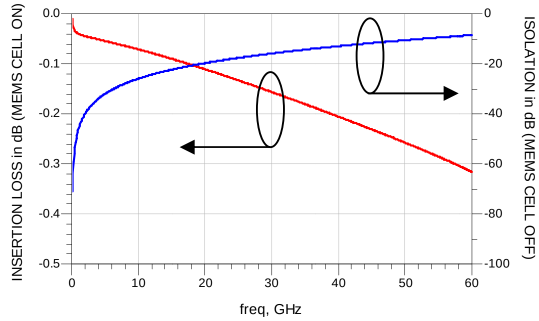


Fig. 4. EM simulation of MEMS Cell in ON and OFF state using FEM

TABLE II
COMPARISON OF SIMULATED PERFORMANCE OF MEMS CELL

MEMS Cell State	Simulator	S21@30GHz in dB	S11@30GHz in dB
OFF	3D	-15.83	-0.277
OFF	2.5D	-17.19	-0.128
ON	3D	-0.157	-21.78
ON	2.5D	-0.318	-27.61

The MEMS SPDT design should be such that after standalone fabrication and test, it can be connected to the dual LNA MMIC simply by removing the probe pads in both the MMICs. Both 2.5D and 3D simulated EM data is used to design the SPDT switch with matching networks at input and output (Fig. 5). For this, circuit simulator is used.

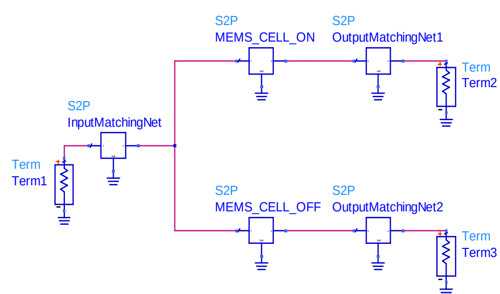


Fig. 5. Schematic of MEMS SPDT switch with matching networks

A T-junction is used to connect the two MEMS cells and input network. The two cells are kept as close as possible and these cells are oriented in such a way that pillar part is towards junction and cantilever part is towards output ends. This ensures that the OFF state cell does not load the circuit with its cantilever acting as open stub. Without any output matching network, the SPDT size is 700 µm in y-direction, additional 355µm increase in switch size is required to make this switch compatible with dual LNA. 2.5D EM simulation is done after addition of each transmission line/component to the switch to keep a check on the overall performance of the switch. Table III summarizes the simulated performance of SPDT at each step.

TABLE III

SIMULATED PERFORMANCE OF MEMS CELL BASED SPDT

Changes in Layout	S21@30GHz in dB	S11@30GHz in dB	S31@30GHz in dB
Two MEMS cell connected in schematic	-0.40	-16.3	-22.5
Two MEMS cell With T-junction only	-0.51	-15.8	-23.4
Input matching network	-0.49	-29.6	-23.5
Long output lines	-0.59	-30.3	-22.9

It is clear that on adding the lines and junctions, the insertion loss has increased to -0.59dB [7]. 3D EM data is also used and simulated in above fashion, with total SPDT layout EM simulation showing, -0.39dB loss with return loss and isolation going better than 20dB. No modification to MEMS series switch structure is done to further improve the performance of the switch in both 3D and 2.5D environment, since the worst results has 0.4 dB margin with specifications. Finally, a resistor is connected to the cantilever end of MEMS cell to the ground to ensure a high potential difference between cantilever part and actuation pad. Value of resistor is kept high and switch is analysed again to check the performance. A 5.6k GaAs resistor with 5µm width is used to eliminate any capacitive parasitic. The full simulation of switch in 2.5D is shown in Fig. 6 with chip layout. The chip dimension is 0.85 × 1.65 mm^2 on 0.1 mm GaAs substrate.

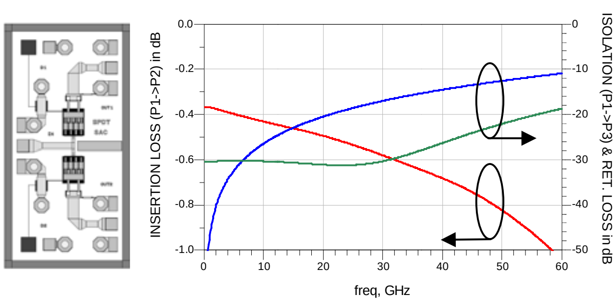


Fig. 6. Micrograph of MEMS based Ka-band SPDT and simulated response in 2.5D solver

III. MEASUREMENT

The measurement of SPDT switch is done on-wafer after the wafer fabrication process. The measured results are with actuation voltage in the range of 70V. The measured results are limited over 25-35 GHz, though being direct contact type, this switch works right from DC [8]. The difference between measured and simulated insertion loss is close to 0.3 dB at 30GHz, and this is due to modeling inaccuracies with respect to pull up & down state of cantilever part. The gap between actuator and lever is not modeled as per the shape taken by cantilever during pull down state.

The fabricated chip and measured results are presented in Fig. 7. The comparison of this switch with other solid state switches are in Table IV.

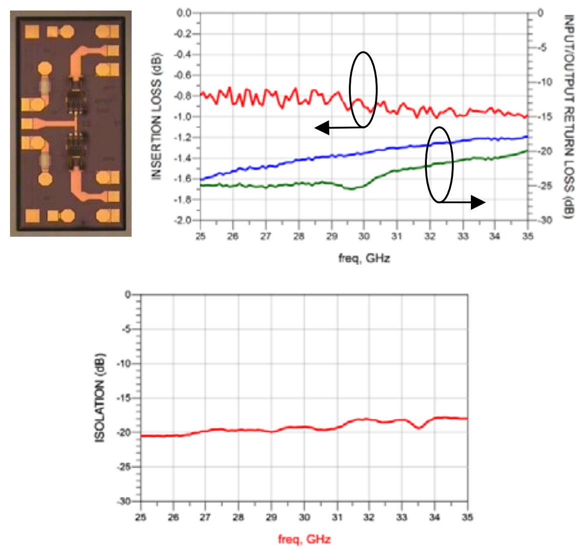


Fig. 7. Photograph of MEMS based Ka-band SPDT MMIC and on-wafer measurement results over 25-35 GHz

TABLE IV

COMPARISON OF SOLID STATE FET & MEMS SPDT ON GAAS

Reference/ Key parameters	[7]	[9]	[10]	This work
SPDT switching element	MEMS	MESFET	HEMT	MEMS
Operating Bandwidth (GHz)	DC-35	20-40	DC-40	Sim: DC-35 Meas:25-35
Insertion loss (dB)	≈ 0.8	< 2	< 2	< 0.9
Chip size (mm^2)	0.8×1.3	1.3×1.3	1.5×1.0	0.85×1.65
Actuation Voltage (V)	90/0	0/-3	0/-1.7	70/0

IV. CONCLUSION

This work establishes a low loss GaAs based MEMS SPDT at Ka-band and gives motivation to single chip solution for redundant Ka-band low noise front-ends. Theoretically, this switch can work linearly even in case of high power redundant stages [11]. This work also opens scope for accurate modeling of MEMS cell in its two states, though here it is demonstrated that for such structures even 2.5D solvers are also capable of predicting performances with little error, thereby reducing the design time considerably as compared to working with 3D solvers. For this work, ADS MOMENTUM is used for EM simulation.

Some critical measurements are still to be done, like IIP3 and dependence of insertion loss and isolation over actuation voltage [11]. These measurements will be done, in test-fixture, for which work is in progress. Packaging of MEMS based SPDT is also to be carried out [12].

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