Design of Transmitter-Receiver for FM-CW Imaging Radar at L-band

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Abstract:

Recently, there has been a growing interest in FMCW (frequency modulated continuous wave) technology based imaging sensors for military and civilian applications. LFM-CW based system has advantage of simple and cost effective processing hardware with a lower cubage than a comparable pulsed SAR. The development of low power L-band FM-CW imaging radar hardware for accurate range measurement is the main focus of this paper.

Key words - FMCW, DDS, PLL-VCO, Phase noise, Loop Filter

I. INTRODUCTION

FMCW technology based radars are emerging to play an important role in small-scale remote sensing applications, such as monitoring and planning of the urban environments and military reconnaissance [1]. An LFM-CW system maintains a high signal to noise ratio by maximizing the pulse length, while transmitting with a lower peak power than a comparable pulsed SAR [2]. Also, the processing hardware is simple which performs an analog "de-chirping" of the signal in which the received signal is mixed with a copy of the transmitted signal. Since the waveform is an LFM chirp, the difference between the transmitted chirp and a delayed copy of itself is a single frequency. These frequencies correspond directly to the slant-range of the target. Thus, the de-chirped signal is a frequency domain representation of the range-compressed SAR image.

The development of low power L-band FM-CW imaging radar hardware for accurate range measurement is the main focus of this paper. The design consideration for FMCW systems is a linear frequency modulation technique that determines the quality of received IF signal. For generating a linear sweep in frequency generally a voltage controlled oscillator (VCO) is used which is a nonlinear active device. Although the VCO based design has advantage of high frequency and wide bandwidth linear FM sweep generation, the nonlinearities in the frequency sweep are very prominent. A direct digital synthesizer (DDS) based FM sweep generation system provides a comparatively lower phase noise and precise linear frequency modulation.

This paper describes a DDS-phase locked loop (PLL) combination of a L-band transmit-receive radar system, whose VCO nonlinearities are controlled by a DDS generated reference signal to make up for a wide band operation and linear frequency modulation. A study of wideband transmitter-receiver design with PLL-VCO combination is done in the paper. The contribution in the design is devising a stable third order loop filter PLL for fast locking and settling time. All simulation results are done in SIMULINK® environment and test results of designed hardware for transmit-receive system are shown in the paper.

II. BACKGROUND PRINCIPLE OF FMCW RADAR

The frequency of the transmit signal increases linearly with time as shown in Fig.1 and is mathematically expressed in the time-domain as follows [3]

$$S_t(t) = \cos 2\pi(f_o t + \frac{1}{2}\alpha t^2) \qquad (1)$$

where, $\alpha = \frac{BW}{T}$ is the FM chirp rate, BW is the FM chirp bandwidth and T is the sweep time.
The received signal is a delayed version of the transmitted signal and is represented as

$$S_r(t) = \cos 2\pi(f_o(t-\tau_o) + \frac{1}{2}\alpha(t-\tau_o)^2) \qquad (2)$$

$\tau_o = \frac{2R}{c}$ being the two way return delay for a target at a range distance R.

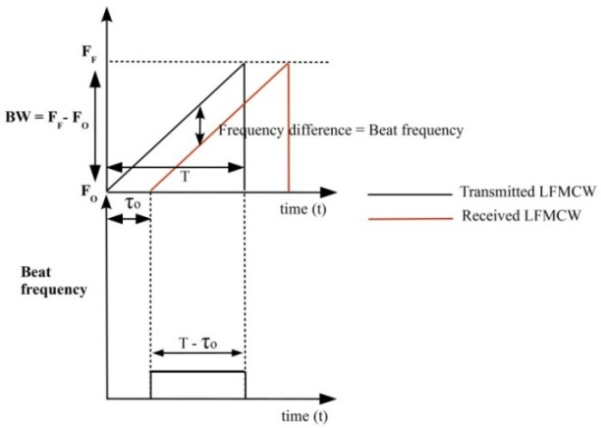

Fig 1. FMCW transmit-receive model.

The transmitted and received signals are then mixed together and low pass filtered to obtain the beat frequency signal corresponding to the delay τ_o which is

$$S_b(t) = \cos 2\pi(f_o\tau_o + \alpha t\tau_o - \frac{1}{2}\alpha{\tau_o}^2) \qquad (3)$$

The second term in (3) represents the beat frequency which is a measure of the range to target and is resolved in the

frequency domain by performing an FFT. The last term is residual video phase error and can be compensated.

III. DDS based FMCW HARDWARE simulation

The complete hardware schematic of a low power L-band FMCW radar using commercial off-the-shelf electronic components is shown in Fig 2. A linear FM sweep of 100 MHz bandwidth with a very low phase noise output is generated using AD 9858 based Direct Digital Synthesizer (DDS) evaluation board.

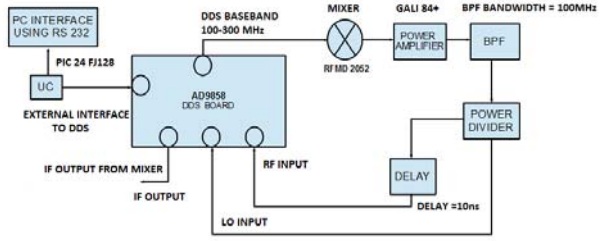

Fig 2. DDS based FMCW transmitter and receiver design model.

The DDS is programmed using a microcontroller which also controls the start/stop time and the bandwidth for generating a linear saw-tooth FM sweep. The FM chirp sweep bandwidth is up-converted to a carrier frequency of 1.5 GHz using a mixer (RFMD - 2052) with integrated programmable PLL/VCO which provides a stable output carrier frequency with low phase noise. The up converted FM chirp is band limited using a band pass filter of 100 MHz bandwidth realized using micro-strip transmission line. The up converted FM sweep signal is time delayed using transmission line based delay line. The delayed signal is mixed with its non-delayed counterpart in the mixer provided in the AD 9858 DDS evaluation board to obtain the beat frequency corresponding to the time delay.

Table 1. Hardware parameters for L-band FMCW radar trans-receiver

Sr.	Parameters	Specifications
1.	FM sweep bandwidth	100MHz
2.	Transmission line delay	10ns
3.	Mixer LO frequency	1.5GHz
4.	Clock frequency for DDS evaluation board	1GHz
5.	VCO frequency range (L-band)	1.5-2.4GHz

In order to understand the behavior of the proposed hardware, a design simulation of the various subsystem blocks is presented in Matlab®Simulink® environ in Fig 3. The simulation design consists of a baseband FM sweep of 100 MHz bandwidth and sweep time of 40 µs. A PLL block as shown in Fig. 6 is modeled for a stable carrier frequency of 1.5 GHz. The baseband FM sweep is up converted to the PLL frequency using a multiplier block. A band pass filter with pass band frequency of 1.5 -1.6 GHz selects the upper side band of the unconverted sweep spectrum. The up converted single sided sweep spectrum is multiplied with a delayed copy of itself to produce a beat signal corresponding to backscatter delay from a range of 2.25 m. A delay of 10 ns is modeled using the delay block. To obtain the beat signal output of multiplier is passed through a low pass filter of cut off frequency 100 KHz. For observing the frequency spectrum, output of each block is sampled at Nyquist rate using a zero order hold. The sampled signal is buffered using a 2048 point buffer block and an FFT of same size is performed.

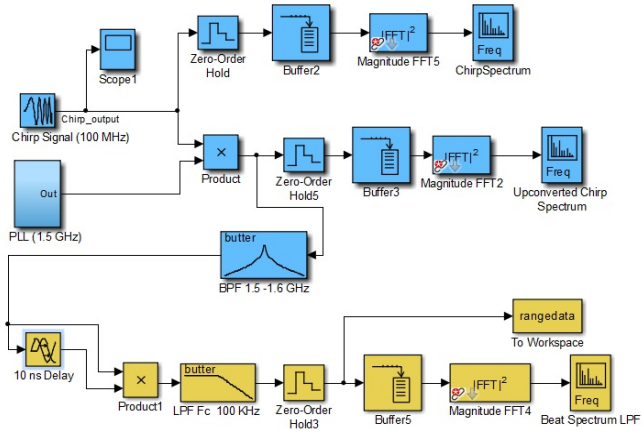

Fig 3. DDS based FMCW transmitter and receiver design model simulated in Matlab®Simulink®.

The theoretically calculated beat frequency is

$$f_b = \alpha\tau = \frac{BW}{T}.\tau \qquad (4)$$

For a BW of 100 MHz, T to be 40µs and considering a delay τ to be 10ns, the beat frequency amounts to 25 KHz. Frequency of beat signal and the resolution are shown in Fig. 4 those are commensurate with the theoretical expectations. The simulink model of PLL-VCO combination and the simulation results is presented in section IV along with the third order loop filter design.

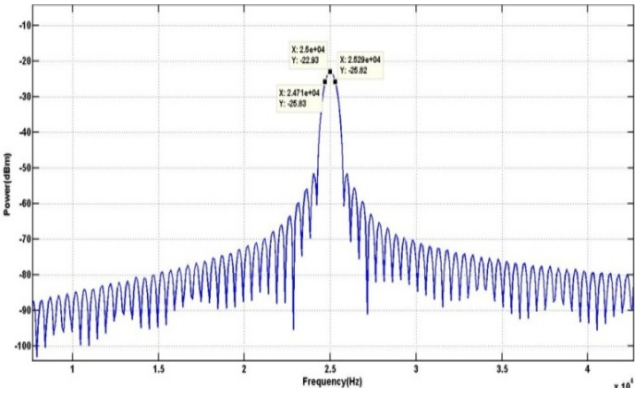

Fig 4. Beat frequency spectrum simulated in Matlab®Simulink®.

IV. THIRD ORDER LOOP FILTER DESIGN FOR PLL –VCO COMBINATION

A PLL is a feedback control circuit that operates by trying to lock to the phase of an input signal by utilizing its negative feedback path [4][6]. A basic form of a PLL consists of three fundamental functional blocks namely phase frequency detector (PFD), loop filter (LF), voltage

controlled oscillator (VCO) with the circuit configuration shown in Fig 5.

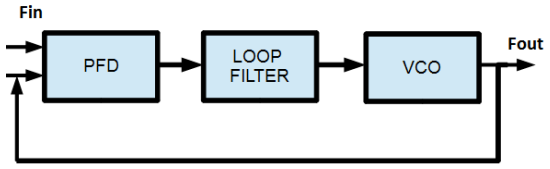

Fig 5. Basic block diagram of components of PLL.

The behavioral model of a charge-pump PLL [8][9] as shown in Fig. 6 is created in Simulink® and studied for its response.

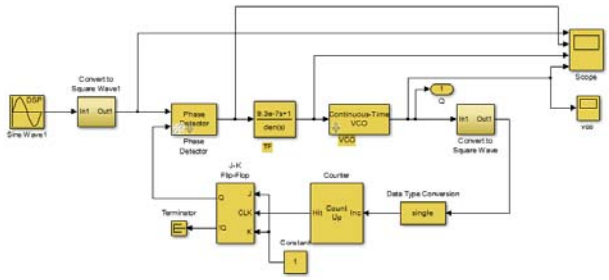

Fig 6. Simulink® model of PLL.

Reference frequency of 4.8 MHz is given as one of the input to PFD, with the other input coming from VCO output as a feedback signal. The feedback frequency is divided down using a counter whose count value is set to 312 to get the output of VCO as 1.5GHz. A third order loop filter is designed which has a settling time of 6µs.

1. Third order loop filter design:

Third order loop filter for the PLL [5][7] is designed and simulated using Simulink® and verified using ADIsimPLL[10] software for its frequency response.

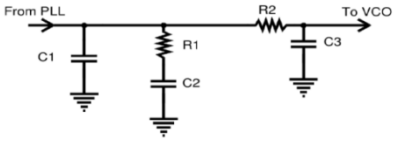

Fig 7. Loop filter configuration.

The design calculations for finding the loop filter co-efficients for a passive two pole loop filter along with a single-pole spur filter shown in Fig 7 are presented. The PLL output natural frequency is [5]

$$f_n = \frac{-1}{2\Pi * t_s * \eta} * \ln\left(\frac{f_a}{f_{step}}\right) \qquad (5)$$

f_{step} = maximum frequency change during a step from one frequency to another, f_a = frequency step after locking of PLL, η = damping factor (0.707 is the typical choice for 45˚ phase margin), t_s = desired time for the carrier to step to a new frequency, I_{cp} = charge pump average current (a nominal value of 1mA is taken for the present design), K_{vco} = sensitivity of VCO. Taking a nominal value of f_{step} as 100 MHz and f_a to be 920 MHz, f_n becomes 1.04MHz**.** The value of loop filter coefficients is found as follows

$$C2 = \frac{Icp * Kvco}{N * (2\Pi * f_n)^2} \qquad (6)$$

N is the feedback divider value, which is a ratio of maximum VCO output frequency to the input reference frequency(channel spacing). For a maximum VCO output frequency of 1.5 GHz and input reference of 4.8MHz, N is 312. The VCO sensitivity/gain is defined as

$$Kvco = \frac{F_{max} - F_{min}}{V_{max} - V_{min}} \qquad (7)$$

V_{max} and V_{min} are the maximum and minimum input control voltages applied to the VCO. F_{max} and F_{min} are the corresponding frequencies obtained at the output of VCO. Putting, $I_{CP} = 1mA$ and $K_{vco} = 30$MHz/V in equation (6), value of $C2$ comes out to be 92pF. Generally, C2 is 10 times $C1$, therefore $C1 = 9.2$pF.

$$R1 = 2 * \eta * \sqrt{\frac{N}{Icp * Kvco * C2}} \qquad (8)$$

From the values obtained above $R1$ is calculated to be 15 kΩ. $R2$ and $C3$ are used to reduce spurs due to reference frequency and their product should be atleast one-tenth the product of $R1$and $C2$ [5]. The simulation result of the Simulink® model of PLL is shown below in Fig 8 for the PFD, loop filter and VCO output. Settling time of the PLL is 6µs as seen from the simulation result.

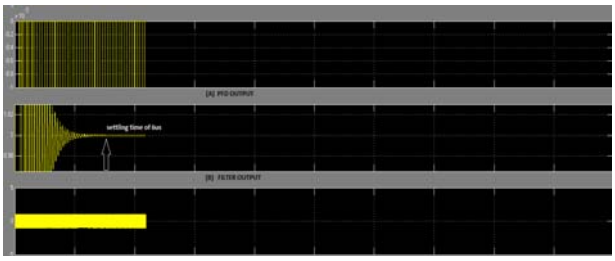

Fig 8. Design results of 3rd order loop filter; (a) PFD output, (b) Loop filter output showing the settling time, (c) The RF output of VCO.

RESULTS

The actual arrangement of the hardware set up is shown in Fig 9.

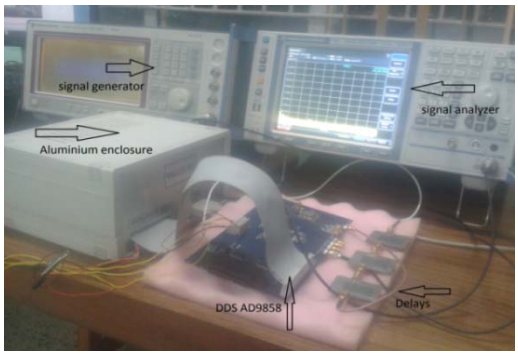

Fig 9. Actual hardware setup for FMCW RADAR trans-receiver.

The reference frequency of 1GHz which acts as the clock frequency to AD9858 DDS evaluation board is generated using Rohde & Schwarz signal generator. The aluminum chassis consists of a PIC 124 FJ microcontroller board, RFMD 2052 mixer/PLL-VCO IC, GALI-84+ microwave amplifiers and transmission line filter. The 100 MHz sweep is generated from DDS (AD9858) evaluation board. The frequency spectrum of the FM sweep along with the up-converted mixer output is observed using Rohde & Schwarz signal analyzer.

Fig 10 shows the FM sweep spectrum of 100 MHz bandwidth and a signal power of -7.8 dBm. The output of the DDS for a single tone frequency at 105 MHz with high spectral purity and low phase noise can be seen in Fig 11. The phase noise at 105 MHz is measured to be -94.67dBm at a frequency offset of 10 KHz. The mixer used in the up conversion of the FM sweep has an inbuilt integrated PLL-VCO for LO generation. The LO frequency of 1.5 GHz generated in the mixer is shown in Fig. 12. The up converted FM sweep shown in Fig 13 has a non linear power spectrum. The integrated PLL-VCO in the mixer is driven by an uncompensated reference frequency source due to which the non linear behavior is observed.

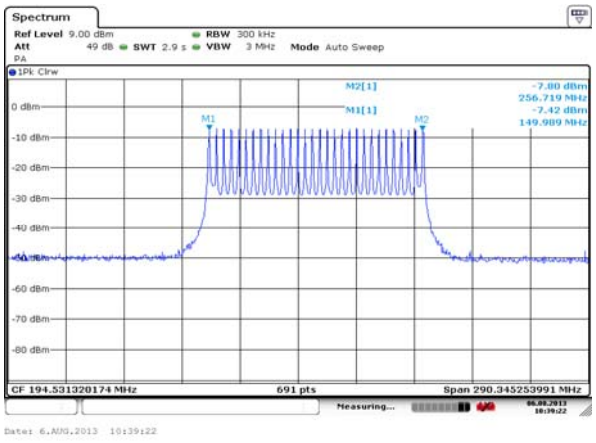

Fig 10. DDS generated FM sweep bandwidth of 100 MHz

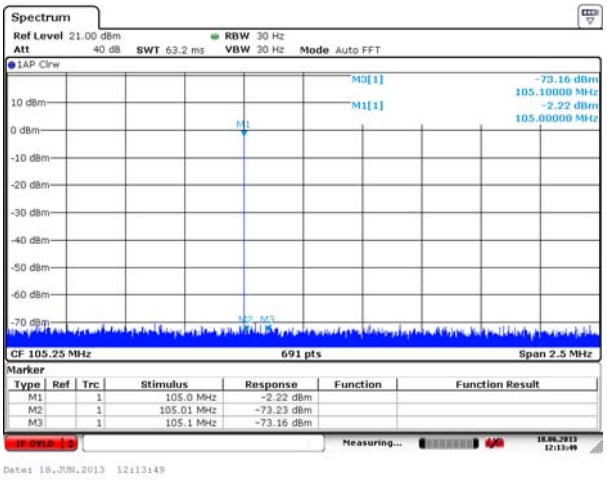

Fig 11. Phase noise measurement for single tone frequency

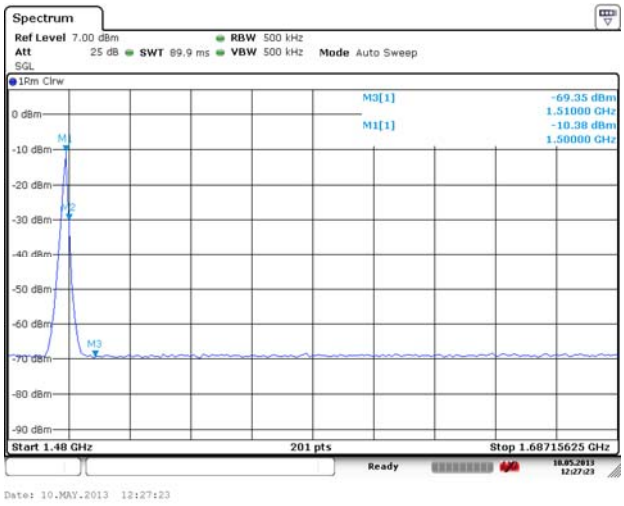

Fig 12. LO frequency of mixer at 1.5GHz.

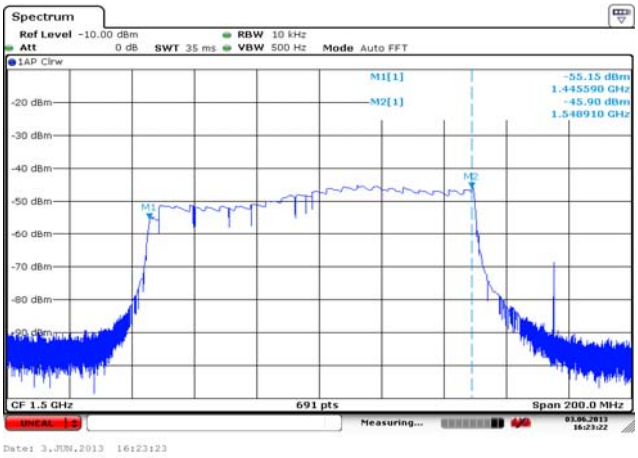

Fig 13. Up-converted upper side band chirp spectrum output of mixer

CONCLUSION

We have shown in this paper laboratory demonstration of a DDS based FM-CW transmit-receive system with a transmission line based delay to measure the specification of a L-band imaging radar. It is observed that for a 100 MHz bandwidth sweep under DDS the phase noise is considerably low. Moreover, we have shown the detailed design of a third order loop filter for the PLL–VCO combination with a low settling time.

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