Reconfigurable Radar waveform and Timing generation Module with target simulation functionality for Exciter applications

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Abstract

This paper presents an FPGA based design of radar waveform and timing generation with BITE functionality for target simulation. These three functions of waveform, timing and BITE generation are integral part of Radar exciter and are very crucial for Radar operation. The hardware is primarily designed for generation of LFM/NLFM waveform, timing and BITE on-the-fly based on the parameters received from Radar controller over gigabit Ethernet link. This design approach is fully reconfigurable for porting other Radar waveforms without any hardware re-spin. The present design is evaluated for existing Radar platform and available as single module with conduction cooled mechanical housing.

Keywords: ***Field programmable gate array (FPGA), Built in test equipment (BITE), linear frequency modulation (LFM), peak side lobe level (PSL), Radar controller (RC)***

I. INTRODUCTION

Pulsed Doppler Radars determine the range of a target using pulse-timing techniques and uses Doppler Effect of the returned signal to determine target object velocity. Different waveforms are employed to enhance the radar performance, in terms of side lobe reduction, pulse compression ratio and overall system SNR.

Pulsed radar waveforms can be completely characterized by carrier frequency, pulse width, Pulse Repetition Frequency (PRF), pulse modulation and modulation bandwidth. Radar design enables the choice of carrier frequency, while pulse width and bandwidth are decided by processing gain and range resolution.

In modern radars the waveform generation and, modulation is performed digitally using FPGA's. This approach provides extreme flexibility of implementation including portability of multiple types of waveforms, fully pipelined digital signal processing and in-system programmability for future system upgrades.

Digital generation methods of frequency modulated continuous wave signals include direct waveform synthesis and frequency synthesis. The signal can be generated directly at Intermediate frequency (IF) or from its baseband components and I/Q modulation done to form the analog IF signal. Subsequently the IF signal is up-converted to Radar operating frequency in analog domain.

In the digital up-conversion (I/Q modulation) the digital samples of LFM waveform at the desired frequency, pulse width and bandwidth are generated offline in MATLAB and stored in FPGA BRAM or external memory. Based on the commands from RC, these waveform coefficients are read, up sampled and multiplied by 60 MHz reference signal generated by FPGA based DDS. Further these samples are band pass filtered and interfaced to DAC for generating LFM chirp at 60 MHz IF.
This waveform is further up-converted to the radar's operating frequency and transmitted.

II. DESIGN APPROACH

The design presented in this paper is part of Radar Exciter receiver which performs the three basic functions of Exciter i.e., Waveform (LFM/NLFM), Timing control and, BITE generation. The other modules include power supply, DDS based synthesizer, up converter, four channel receiver. The system level block diagram is shown in the Figure1

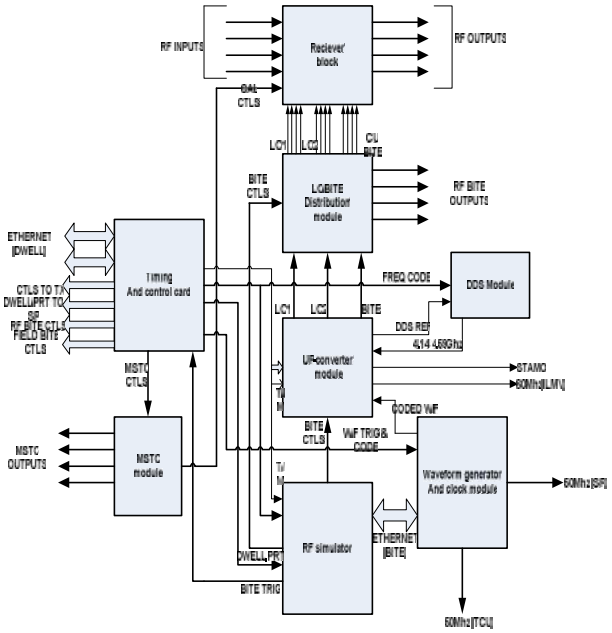

Figure1. Exciter-Receiver System block diagram

The hardware for this module is based on Xilinx kintex7 series FPGA. Provision is made for two gigabit Ethernet links for connectivity to RC with external memories DDR2 and Flash for storing the waveform coefficients. High speed 1.2Gsps DAC is provided for generating LFM chirp waveform at 60 MHz IF. Other components include on board temperature sensor for temperature monitoring and transceivers (RS422/TTL) for status monitoring and control signal generation for other Radar sub systems. The board level block diagram is shown in the Figure 2. The entire module is designed for conduction cooled chassis and, for adaptability to harsh operating environments, environmental stress screening (ESS) tests are done.

1. Waveform generation:

Linear frequency modulation (LFM/NLFM) waveform has been chosen for the present application. A long pulse can have spectral bandwidth as a short pulse if the long pulse is modulated in frequency or phase. If the frequency increases linearly from f1 to f2 over the duration of pulse (up chirp) and, if the frequency decrease with time then it is down chirp.

The LFM up-chirp instantaneous phase can be expressed by,

$\Psi(t) = 2*\pi*(f0 * t + \mu * t^2/2), -t/2 < \tau < t/2$ ……..(1)

Where, f is the radar centre frequency, $\mu = 2\pi B/\tau$ is the LFM coefficient

Thus the instantaneous frequency is given by:

$f(t) = (1/2*\pi)*d/dt$ …….. (2)

$(\Psi(t)) = f0+\mu*t, -t/2 < \tau < t/2$ …….. (3)

Similarly, the down-chirp instantaneous frequency is given by,

$f(t) = (1/2*\pi)* d/dt(\Psi(t)) = f0-\mu * t, -t/2 < \tau < t/2$…(4)

The linear frequency modulation coefficients are computed as per above equations. The sampling frequency is chosen corresponding to the bandwidth of the waveform to be generated. Figure3 and 4 shows plots of LFM waveform at base band level. Main advantages of LFM waveform are insensitivity to Doppler shifts, high range resolution.

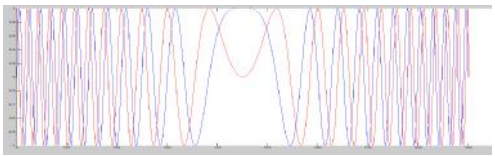

Figure3. I-Q samples generated at Base band level

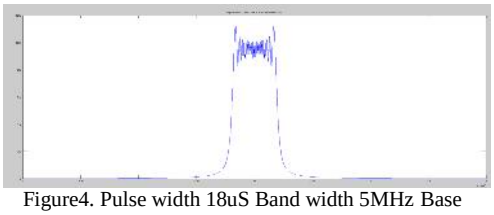

Figure4. Pulse width 18uS Band width 5MHz Base band spectrum view

2. UP-conversion to IF stage

The basic band pass signal representation is given by

$X(t) = X_I(t) \cos 2\pi f_0 t - X_Q(t) \sin 2\pi f_0 t$ …… (5)

Where $X_I(t)$ and $X_Q(t)$ represents I and Q coefficients respectively, f_0 is the radar centre frequency at IF level. Cosine and sine components of f_0 are generated by FPGA based DDS. Modulation is performed using Xilinx system generator design flow. After modulation output samples are band pass filtered in FPGA and fed to Digital to analog converter.

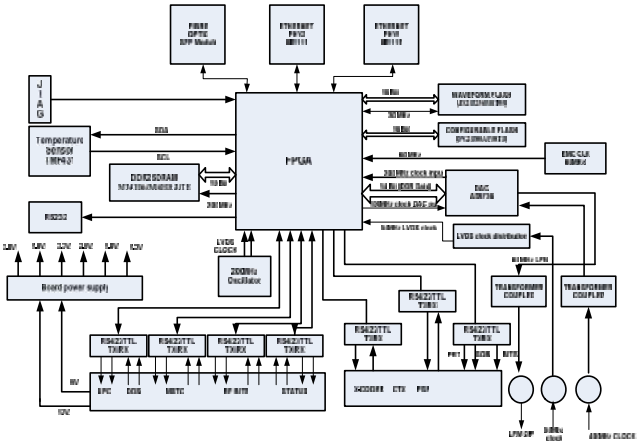

Figure2. Board level block diagram

3. NLFM waveform significance

LFM matched filtering results in range side lobes. These side lobes are often undesirable because they mask small targets or may they be mistaken for targets themselves. NLFM matched filtering has better detection and estimation characteristics than LFM with side lobe control. The phase modulation function for NLFM is designed using Taylor series correction. It is given by

$$\Psi^{NLFM}(t) = \pi\beta t^2/\tau - \pi\beta\tau \sum_{n=1}^{N} K_n/\pi n \cos(2\pi nt/\tau) \ldots (6)$$

Coefficients are calculated using above equations and up conversion is performed. So at the receiver no weighting function (windowing) is required. This results in peak side lobe level is decreased to -40db. NLFM waveform is also validated using MATLAB. Similarly other waveforms can also be ported without any modification in the present hardware.

4. Timing generation:

In the present design, FPGA receives 50MHz master clock from synthesizer which is used as reference for timing generation for various radar sub systems. Radar controller sends the dwell parameters scheduled on a dwell to dwell basis to the FPGA over Ethernet link. Dwell parameters include type of waveform (LFM/NFLM), pulse width, PRF,

bandwidth (5/10 MHz), number of pulses within dwell along with information to SP and other modules.

Complete custom UDP/IP hardware stack in VHDL is developed and used in FPGA to receive the dwell and bite parameters. Waveform parameters are passed onto the waveform generation module and, timing information is used to generate Dwell, PRT and other control signals. A tight hand shaking mechanism is employed between RC and FPGA to maintain synchronization. These timings generated by the FPGA are used to synchronize the waveform transmission with all the subsystems of the radar.

5. BITE generation:

Modern radars provide target simulation mode to validate various sub systems of Radar whenever it is offline. BITE targets generated act as echo returns from real targets. There is provision of generating targets with or without Doppler hence both stationary as well as fixed targets can be emulated.

The provision of BITE mode of operation is made in the present hardware by including separate dedicated Ethernet link to the RC. BITE parameters include number of targets with target range, spacing between targets, approaching or receding targets with Doppler and attenuation values for sum, azimuth, and elevation channels. These parameters are received by the FPGA, targets generated during pulse off time.

In addition to target BITE generation this Ethernet link is also used to send status information to RC. All other subsystems send status information over dedicated RS422/TTL lines to this module, and the status information is consolidated and sent to RC on regular basis.

III. IMPLEMENTATION ARCHITECTURE

The entire design is based on single Xilinx Kintex7 series FPGA which is manufactured using low power 28-nm process technology. It provides low cost, low power 1.0V core supply, 900 pin FBGA package, with around 350 high range (HR) I/O's supporting(3.3V to 1.2V) and high performance (HP) I/O's (1.8V to 1.2V). It has Block RAM memory of around 25Mbit with 1540 DSP48E1 slices and 406720 logic cells. Based on 6-input LUT architecture provides implementation of wide input combinational logic functions.

The functional block diagram is shown in the Figure5. The front end interface to RC is gigabit Ethernet link where all the parameters are communicated over UDP/IP link. FPGA interfaces to external PHY chip in GMII mode, implements the MAC layer functionality as well as custom UDP/IP stack in VHDL. The dwell and BITE parameters are written into dedicated BRAM memories. Based on the handshaking mechanism employed, acknowledgement is sent to RC for every dwell and BITE packet. Timing generation is initiated by RC by sending dwell start packet and the corresponding dwell parameters are read from BRAM memory and loaded to Timing generation module. The waveform coefficients are generated in MATLAB for the required pulse width, bandwidth and stored in BRAM memory. Presently only LFM/NLFM waveforms are implemented. These coefficients are read from BRAM and up-sampled, and multiplied by sine and cosine signals at 60 MHz in digital I/Q modulation module. FPGA based DDS is used to generate the sine and cosine signals.

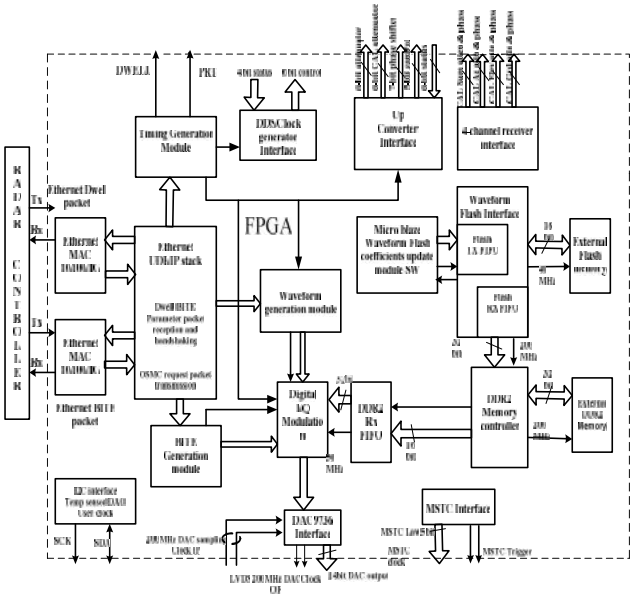

Figure5. Functional block diagram

The output samples are band pass filtered and fed to DAC for analog LFM chirp generation. This LFM chirp signal is given to external up converter module for conversion to Radar frequency and transmitted.

Provision of storing multiple Radar waveform coefficients in hardware is done by writing these coefficients in external 32MB flash memory. On power-on these coefficients can be copied into external DDR2 memory for faster memory access. From DDR2 coefficients can be buffered in FIFO and the same process of I/Q modulation can be done. Separate FSM's are implemented for both Timing and, BITE generation. The process of updating the waveform coefficients into external Flash memory is done in software using embedded Micro blaze microcontroller. PC based GUI used to interface to RC for receiving dwell and BITE parameters on Ethernet link. The output LFM waveform at 60Mhz IF is observed in spectrum analyzer and timing on CRO.

Additional glue logic implemented to interface to other modules of the exciter receiver. These modules include (i) DDS based synthesizer for 50 MHz timing reference clock and, 400 MHz sampling clock for DAC and LO1 for up conversion, (ii) Up converter module takes the 60 MHz LFM, LO1 and generates LO2 and further converts it to C band signal for transmission.

IV. TEST RESULTS

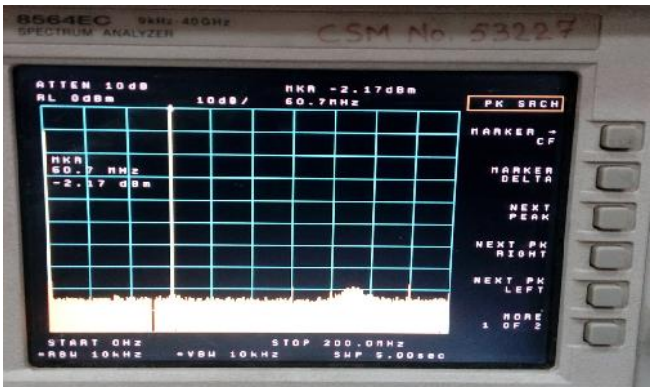

Figure6.SFDR measurement using spectrum analyzer (400MHz-clk input, 60MHz output) 60MHz level=-2.17dBm and next highest peak within Nyquist zone is @ 180MHz= -76.17dBm.SFDR=74dBc

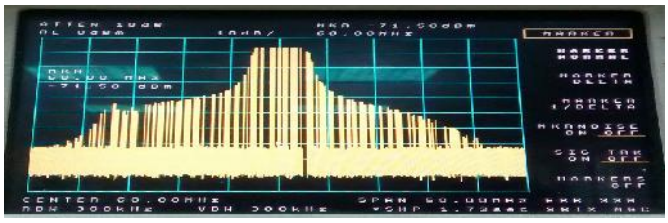

Figure7. IF spectrum for 18uS Pulse width 5MHz Band width

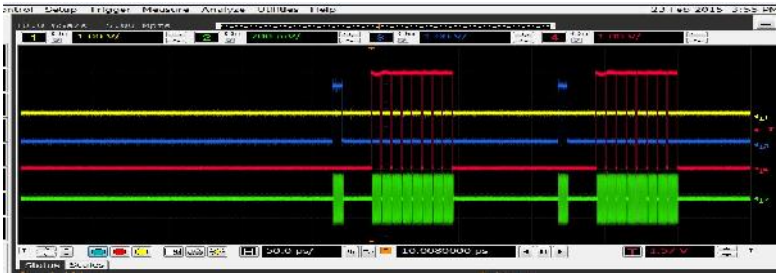

Figure8. Multiple targets generated for 10km range 300m spacing

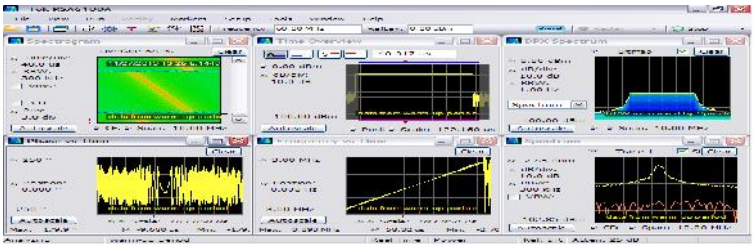

Figure9. Real time spectrum view of IF output (LFM)

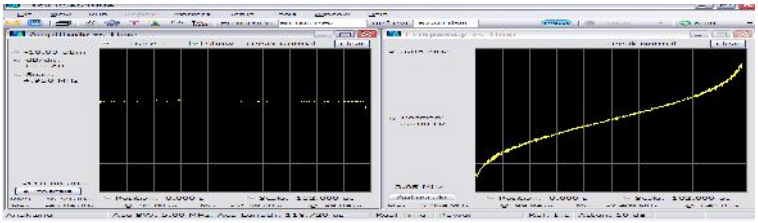

Figure10. Real time spectrum view of IF output (NLFM)

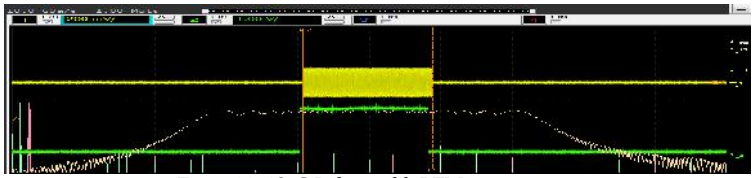

Figure11. 18uS Pulse width LFM scope output

V. CONCLUSION

The design presented in this paper implements all three basic functions of Radar exciter waveform, timing and, BITE generation in a single FPGA based module. This module is a good form fit replacement for other OEM vendor solutions offered as three separate modules for the same functionality. It addition to this it can be easily re-configured to port different Radar waveforms with IF frequency support upto 120Mhz.The entire module is housed inside a conduction cooled enclosure and it is designed to meet rugged operating conditions of Military Radars.

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