Design & Development of 1.5KW, L band Pulsed Power Amplifier

Pankaj Gupta , Prakash S.P, Sudip Kumar Murmu, Ambethkar.K
Central D&E-RF Components, Bharat Electronics Limited (BEL),
Jalahalli Post Office, Bangalore – 560 013.
pankajgupta@bel.co.in, prakashsp@bel.co.in

Abstract :

In this paper, the design aspects of 1.5KW L-Band Solid State Pulsed Power Amplifier operating in the frequency band 1.25GHz to 1.35GHz using LDMOSFET is described. This 1.5KW module is the basic building block of 6KW Power Amplifier with 150us at a 10% duty cycle. Four such Amplifiers are combined to get 6KW power output using 4-Way combiner. This paper also describes design of 500W Power Amplifier based on LDMOSFET device. The input, output matching circuits are simulated and realized on low loss PCB RF substrate. The measurement was carried out over this band for verifying the parameters.

The main application of this module is in Surveillance RADAR. This paper elaborates on critical requirements, the design aspects, implementation & engineering of Power Amplifier.

Key Words : LDMOSFET, PCB, CW, KW,SSPA, GaAs, GHz, VDD, DC, PAE,SPI

I. INTRODUCTION

The generation of high power microwave pulses is fundamental to the operation of various systems ranging from radar to particle accelerators, from communications systems to cancer treatments. In the past such systems have depended on tube amplifiers or cavity sources. With recent advances in solid state transistor technology ever increasing power levels are achievable without the need for turning to travelling wave tube technology and its inherent disadvantages.[1] This paper reviews the design of a 1.5kW amplifier operating in the L band for radar. In Section II describes Pulsed versus CW and experimental results on the 1.5 kW SSPA are in Section VIII .

II. PULSED VERSUS CW AMPLIFIERS

In terms of the design of solid state amplifiers the distinction between pulsed and Continuous Wave (CW) operation is not as obvious as would first appear. Transistors are available capable of handling hundreds of watts of RF power, but only for relatively short pulses and low duty cycles. Once the pulse width exceeds the order of 300µs, or the duty 20% the selection of the transistor becomes limited to various suppliers of CW devices. These two limits are exclusive, i.e. a system operating with 200us pulse widths will typically have a duty cycle of <3%, and a system with a duty cycle of 20% will be operating with pulse width of the order of 10 µs.

An amplifier operating with RF pulses, above the limits given above, will still have different design criteria to a CW amplifier, (mainly regarding the power supply and thermal management), however for the transistor selection the power levels available are reduced by as much as a factor of 6.

The power limitation in the devices is currently as a result of the thermal properties of the devices. Modern high power transistors consist of a number of cells combined in parallel. For correct thermal operation the RF (Radio Frequency) current must be shared equally between the cells, otherwise just like the weakest link in a chain, the first cell to fail will destroy the whole transistor. In each cell the actual transistor junctions are located on or near the surface, and the immediate surroundings have a relatively large thermal capacity, hence the ability to operate at high power levels for short periods of time, (the junction temperature does not rise instantly with peak RF current)[2].

For pulsed applications transistors are generally biased in class C. In this mode the transistor is biased off in the DC state and relies upon the RF pulse to ‘switch’ the transistor on. This produces a non sinusoidal operation as the transistor is only conducting for less than half a cycle, however the tuned nature of the output circuit and the stored charge of the bias network provide a more symmetrical RF output. In our design device is biased to class AB saturated mode as this gives better lineaity, good efficiency, good pulse parameters[3].

Most CW FET or MMIC amplifier devices can be used for pulse with drain or gate pulsing, but not all pulsed amplifiers can be used as CW. Pulsing the amplifier on/off reduces DC power dissipation, which means that it operates at a cooler temperature. The operating Pulse width also metter the hotness of the device. Because pulsed amplifiers run cooler, they often can provide higher power and efficiency compared to similar CW amplifiers. Pulsed amplifiers require special power supplies to maintain the DC bias point during the pulse; often large charge storage capacitors are needed. For very short pulses, you need to consider the bandwidth of the amplifier, so that it maintains the pulse shape.

III DESIGN REQUIREMENT

Table 1. Specification :

Parameter	Requirement
Frequency Range	1.25 – 1.35 GHz
Peak Output Power	1.5 kW (61.8 dBm) min
Pulse Width	4 -150us
Duty Cycle	10% max
Drive level	50dBm min
Pulse Droop	0.4dB max at 150us
Rise Time & Fall Time	<200ns
Harmonics	-25 dBc min.
Supply	50V DC
Temperature Range	-20 to +55ºC
Interface	SPI

IV. DESIGN APPROACH

The output from the previous Driver stage is split into four by using two 90 degree Hybrid couplers. Each output is fed to 500W basic Power Amplifier stages, with a gain of 15 dB and output of minimum 500Wpeak operating over the full band. PA module receives all bias and supply through Bias card which has provision for capacitors, in-rush current protection, current sensing and thermal sensor[3],[4].

The outputs of all 4 PAs are combined using combination of 2way 90 degree Hybrid couplers to get the 1.5 KW min Peak Power over the full band. This outputs is passed thro Circulator (10KW/300W) and the third port is terminated with 1KW termination.

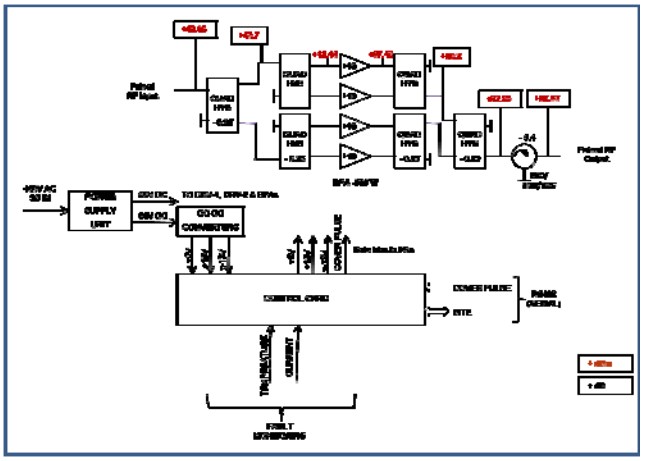

Fig. 1 Block diagram of 1.5KW SSPA Module

The Power Amplifier has two separate gate and two drains which are two separate transistors that are thermally independent. These two transistors are interconnected It has good advantage of good VSWR and system reliability.

The power amplifier design portion is a straightforward implementation using a balanced configuration. Identical low loss surface mount 3dB hybrid couplers are used for the divider and combiner. The balanced configuration provides good isolation between both RF transistors which improves stability. Additionally, balanced amplification provides better input and output return loss when compared to a single ended transistor since reflected power is absorbed by the load in the decoupled coupler port. The 500W transistors have internal matching in conjunction with printed external matching optimized for pulsed operation between 1.25 – 1.35 GHz. The transistor design represents an optimal balance between gain, output power, bandwidth, stability and efficiency.

A block diagram of the 1.5 KW L-band SSPA is shown in Figure 1. The overall gain is more than 12dB which is achieved by parallel amplification of four 500W amplifiers modules which are combined. A four way power divider/combiner consisting of 2 levels of two Hybrid couplers are used to excite and collect power from the four parallel output stage transistors.

PHASE TRACKING

Amplitude and phase tracking is the difference among the power output and relative phase of the 4 Power Amplifier modules at the same frequency In order to achieve good amplitude and phase characteristics. microwave high power transistor being used must have excellent similarity as well as the fine matching circuit and testing system and manufacturing precision[5] .

V. 500W PA MODULE DESIGN

The heart of the SSPA is the 500W amplifier module. The impedance matching network of this Power Amplifier is constructed using microstrip circuit on teflon substrate-RF64 from Taconic incorporating impedance transformation section[6]. Due to tolerence in the fabrication there is some error which was required to to corrected during testing tuning. A photograph of the 500W amplifier module is shown in Figure 2 and measured test result for 500W module is in fig.3.

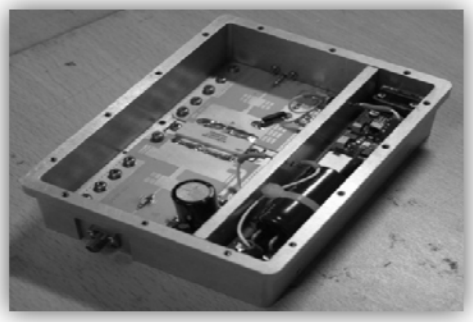

Fig. 2 Photo of 500W Amplifier Module

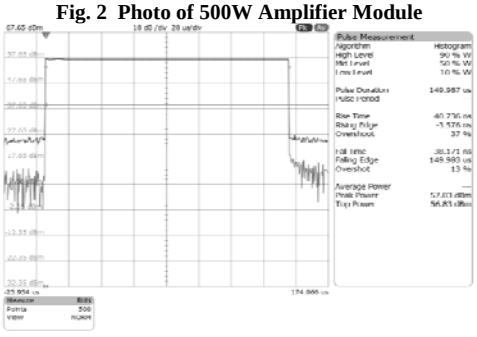

Fig. 3 : Pulse Power Measured on R&S Power Sensor at 1.25GHz with 150uSec Pulse width & 10% Duty Cycle for 500W BPA Module.

VI. DC ENERGY DELIVERY

1.5KW PA module contains four 500W LDMOS transistors. To allow for circulator and combiner losses, each module is designed to operate at approximately 500W per transistor min. . Therefore, with a 50V DC supply voltage and assuming a worst-case efficiency of 40%, each transistor draws average current of 2.5Amps during the pulse amplification. In order to achieve the specified rise time, this means the current into each transistor must rise from zero to 2.5Amps in less than 200nanoseconds. This current is delivered to the transistor through an inductance, L, which decouples the RF path from the DC supply. Thus, the value of L is critical – it must be large enough to properly decouple the RF output from the DC supply, but small enough to permit the transistor current to reach 2.5 amps and the transistor drain DC voltage to stabilise within the required rise time. The optimum value of L was determined and implemented as a printed track on the PCB to ensure perfect symmetry and repeatability in manufacture.

In addition, very careful selection and placement of bypass and storage capacitors was required to produce the minimum possible supply impedance from DC to larger than 100MHz. This wide-band supply bypass avoids any AM ringing or overshoot on the supply and hence on the RF pulse. A very low impedance electrolytic capacitors with value 1499uF calculated based on droop requiremetns, was splitt into 470uF and 1200uF. These are fitted on both RF PCB and on bias PCB which is mounted on the side of the PA module, arranged so as to minimise the inductance between the energy storage and the transistors[7].

VII. CONTROL UNIT DESIGN

The SSPA is controlled and monitored by microcontroller based Control Cards-Master Control Card & Slave Control Card. Master Control Card is placed in RF Driver Unit(external) and Slave Control Card is in 1.5KW PA Unit. Master Control Card & Slave Control Card uses Serial Peripheral Interface (SPI) for data transfer between each other. This reduces the interconnection cables between the Control Cards.

Control Card, switches ON the PA modules 1us before the RF pulse and switches OFF 1us after the RF pulse. This switching ON and switching OFF of the PA modules depends upon the Cover Pulse. The Cover Pulse is received from the Exciter unit in RS422 format.

The Control Cards protect the SSPA from Over temperature and Over current (Over Duty) faults. Temperature and current sensors are provided for each Driver modules and each PA modules. These sensors give output in terms of DC voltages which are given to the Control Cards. When these voltages exceed the set limit, the particular PA module is switched OFF. The faults are indicated using LEDs in Control Card as well as front panel of the SSPA.

The Gate voltages, Vg of the devices inside the PA modules are also monitored. If the device of any PA module fails, then Vg of the device becomes 0V. And this is indicated using LEDs.

The SSPA is also protected from high VSWR. The coupled reflected RF signal is fed to a RF detector. This detector converts the RF voltage into dc voltage. This voltage is amplified and fed to Master Control Card. If this dc voltage is more than the safe limit then high VSWR fault is generated. As a result, the RF input signal is attenuated and the Drivers & PA modules are switched OFF. There is provision for BITE i.e. health status of the SSPA. The Master Control Card receives the health status of 1.5KW PA Unit from Slave Control Card through SPI and stores it. Then it sends the SSPA health status to the Radar Controller when it receives the status request. This status is sent in RS422 format.

Thermal Consideration :

Maintaining as low a junction temperature as possible in the transistors, is key to achieving maximum output power and device reliability. Thermal performance could be improved by soldering the device to the mounting base but this practice stresses the transistor thermally and makes manufacture and maintenance more difficult. The transistors are bolted directly to the module heat sink, with no barrier metals. It is essential that as high a polished finish as is possible is made under the devices for intimate metal to metal contact. The power modules are housed in aluminum enclosure, which is mounted on cold plate with channel running across the width of the module. The entire module is machined from the solid to ensure optimum heat transfer from the LDMOS, which are mounted directly to the inside surface of the cold plate which supplies chilled liquid.

VIII. EXPERIMENTAL RESULTS

The modulated input from Signal generator which is internally modulated at a pulse width of 150us and duty of 10%, fed to this SSPA through driver Amplifier. Cover pulse is synchronized with Signal generator. Peak power of more than 61.8dBm(1.5KW) is measured at output. Output RF power pulse shape of this Power Amplifier module is shown in Fig-5-12. The assembled 1.5KW module photograph is shown in Fig.4.

IX. CONCLUSION

We had successfully designed and tested the performance of 1.5 KW L-Band Solid-State Amplifier over the full band. Few numbers are fabricated and tested for repeatability. This PA was integrated with system and checked for performance. This SSPA achieves high reliability, enhanced performance which are required for RADAR Transmitter and can replace existing system using TWT amplifier.

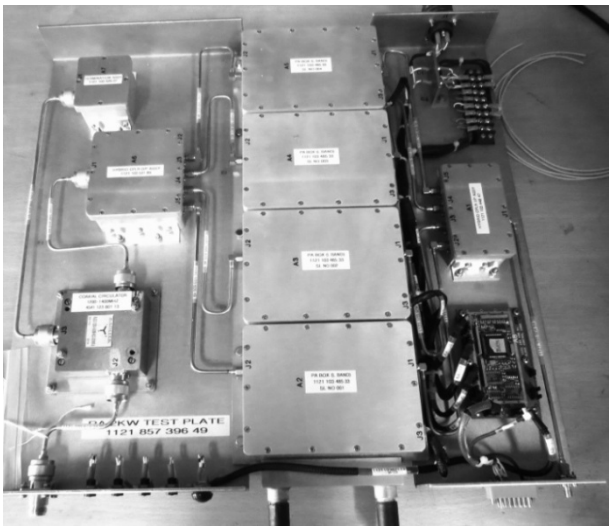

Fig. 4. Photo of 1.5KW SSPA Module

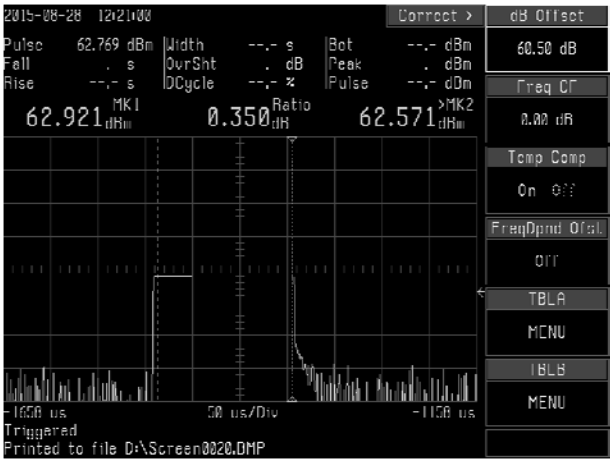

Fig .5 : Pulse Power Measured on Boonton Power Meter at 1.25GHz with 150uSec Pulse width & 10% Duty Cycle. Measured Peak Power 62.92 dBm with droop of .35dB.

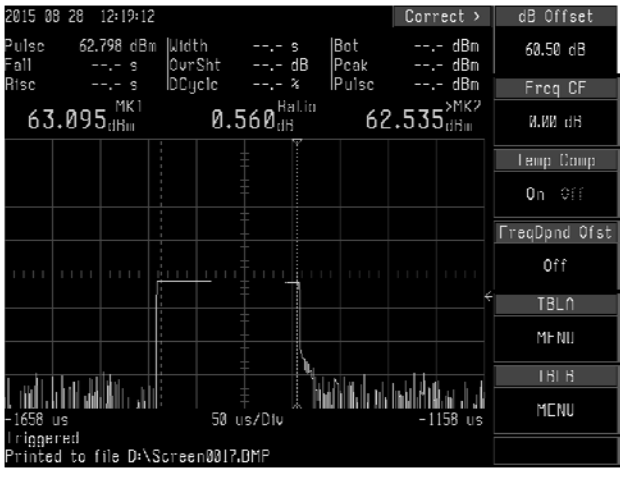

Fig .6 : Pulse Power Measured on Boonton Power Meter at 1.35GHz with 150uSec Pulse width & 10% Duty Cycle. Measured Peak Power 63.09 dBm with droop of .56 dB.

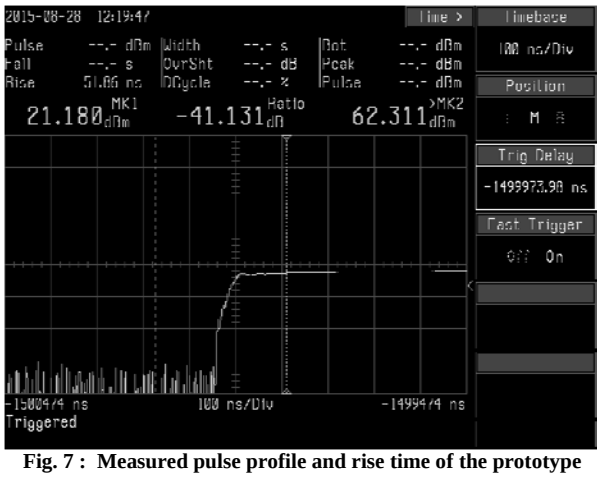

Fig. 7 : Measured pulse profile and rise time of the prototype amplifier with peak power of 62.8 dBm. Measured rise time 51nSec.

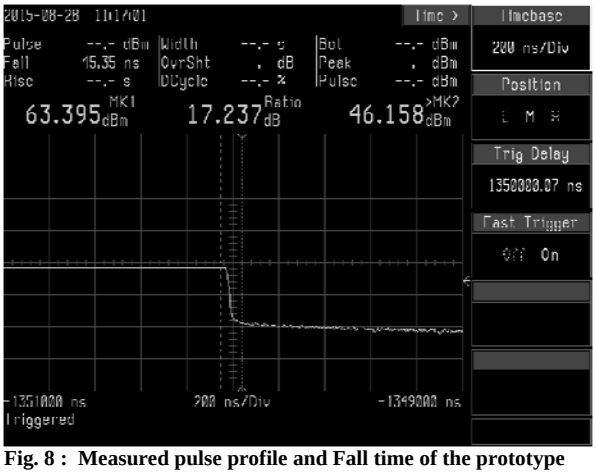

Fig. 8 : Measured pulse profile and Fall time of the prototype amplifier with peak power of 62.8 dBm. Measured fall time 46 nSec.

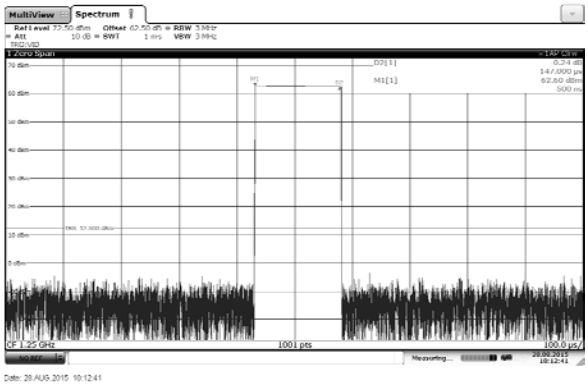

Fig .9 : Pulse Power Measured on R&S FSW8 Spectrum Analyzer at 1.25GHz with 150uSec Pulse width & 10% Duty Cycle.

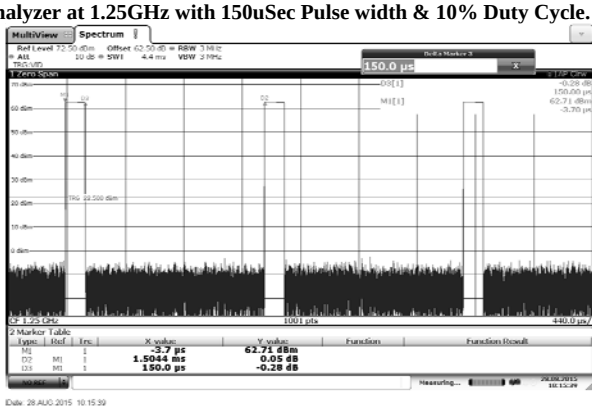

Fig. 10 : Pulse Power Measured on R&S FSW8 Spectrum Analyzer at 1.25GHz with 150uSec Pulse width & 10% Duty Cycle.

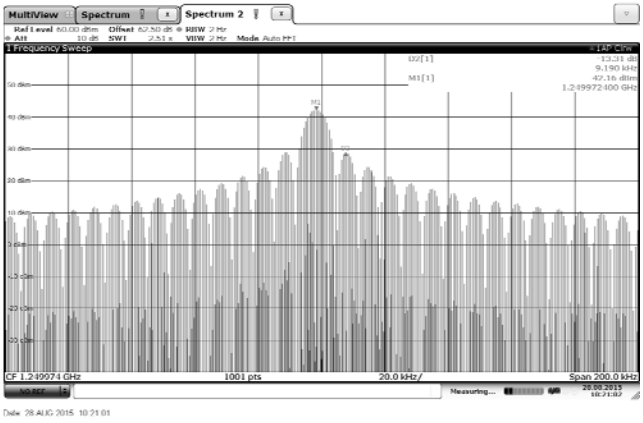

Fig. 11 : Line spectrum of final LRU with 62.8 dBm output power Measured on R&S FSW8 Spectrum Analyzer at 1.25GHz with 150uSec Pulse width & 10% Duty Cycle.

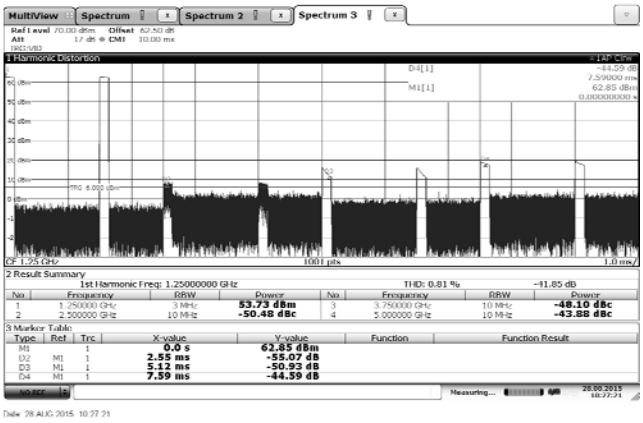

Fig.12 : Harmonic Measurement with R&S FSW8 Spectrum Analyzer at 1.25GHz with 150uSec Pulse width & 10% Duty Cycle. 2nd H 50dBc & 3rd H 48dBc down.

ACKNOWLEDGMENT

The authors would like to thank Mr. Philip Jacob ED, Central D&E, Bharat Electronics Ltd, Bangalore Complex for his continuous support, encouragement and for granting permission to publish this work. We also thank Mr. Shantha Kumar L, AGM (Retired), Mr. Hari Kumar, Sr. DGM, Central D&E-MWC, Ms. Kalyani Murthy, AGM, Central D&E-RFC for their support extended to this work. Authors would also like to mention the contribution by Mr. N Suresh (GM/NS2) and PDG group in providing all the technical support for PA housing and thermal analysis. The authors wish to acknowledge NXP-Semiconductors for their support.

REFERENCES

[1] A. Wood, C. Dragon, W. Burger, "High Performance Silicon LDMOS Technology for 2 GHz RF Power Amplifier Applications", *IEDM 1996*, pp. 87-90 (1996).
[2] H.F.F. Jos, "Novel LDMOS Structure for 2 GHz High Power Basestation Application", *Eu. Micr. Conf 1998*, pp. 739-744 (1998).
[3] F. van Rijs, "Status and trends of silicon LDMOS base station PA technologies to go beyond 2.5 GHz applications", *RWS 2008*, pp. 69-72 (2008).
[4] H. Kim, Y. Jeon, J. Lee, S. Lee, and S. Nam, "A high efficiency power amplifier using multilevel digital pulse modulation," *Microwave and Optical Technology Letters*, 51, pp. 1921-1924, 2009.
[5] M. Skolnik, *Radar Handbook*, and McGraw Hill, 2008, Third Edition.
[6] F. Schweirz and J. J. Liou, *Modern Microwave Transistors: Theory, Design, and Performance*, John Wiley and Sons Ltd, 2003.
[7] P. Colantonio, F. Giannini, and E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, John Wiley and Sons, Ltd,2009.
[8] J. Dhar, R. K. Arora, S. K. Garg, M. K. Patel and B. V. Bakori, "Performance enhancement of pulsed solid state power amplifier using drain modulation over gate modulation," in *Proc. International Symposium of Signals, Circuits and Systems*, Iasi, Romania, 2009, pp 1-4.

BIO DATA OF AUTHORS

Pankaj Gupta received his B. Tech. in Electronics from Awadh University in 2003 and joined Bharat Electronics in the Power Amplifier Core Design Group in 2006. Presently working as a Deputy Manager in C-D&E- RF Components Core Group. His work includes design & development of RF Power Amplifiers from V/UHF to S-Band for various power level which is used in communication radio, Jammer and RADAR application. Also involved in Transmitter module, Passive RF modules, RF simulation, Power Amplifier Linearization Technique, High Power Pulsed Power Amplifier Design.

Mr. Prakash S.P. graduated from PDA College of Engineering, Gulbarga in 1990. He joined Bharat Electronics, Bangalore-Broadcast & Tele Vision division in 1991, worked on Power Amplifiers, diplexers, IF/RF modules for FM Radio, TV transmitters & Satellite Receivers. Currently he is in Central D&E-RF Components group, where he is involved in design & development of RF & MW Power Amplifiers, transmitter modules & related RF sub systems in various power levels and up to S-band for Communication Radios, Radars & Accelerator applications.

Mr. Sudip Kumar Murmu received his B.E degree in Electronics & Telecommunication from Bengal Engineering and Science University, Shibpur (WB) in 2008 and M.E with Microwave Engineering as specialisation from Jadavpur University, Kolkata (WB) in 2010. He joined Bharat Electronics Limited (BEL), Bangalore as Probationary Engineer in 2010. He is presently working as Senior Engineer in RF Components (Central-D&E). He is involved in design & development of Power amplifiers, RF & MW subsystems and microcontroller based control systems.

Mr. Ambethkar K graduated in the stream of electronics and communication from Sree vidya nikethan college of engineering Tirupati(AP) in 2011, and joined Bharat Electronics in 2013. Presently he is working as a Deputy Engineer in Central D&E-RF Components Group. His work includes design & development of RF Power Amplifiers & related modules for Jammer application, High Power Pulsed Power Amplifier for radar application.