Passive Channel Processing In Radar Systems

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Abstract

This work deals with the signal processing aspect of passive channel by suggesting an algorithm for passive channel processing, on the basis of the input and desired output. The simulations are carried out by developing a Simulink model and later, code development is done using a hardware description language.

Keywords *- Passive channel, filtering, target, model, processing.*

I INTRODUCTION

Target tracking has been an area of interest and an active research area from the recent past. There are three problems associated with classical target tracking: detection, association and estimation. Detection pertains to the determination/presence of a signal in noisy environments. Association pertains to the assignment of a number value to the target, or assigning a deterministic nature to the random values obtained from the detection phase data. Estimation of a target implies using the different available target models to zero-in on a hypothesis of action. Here, the hypothesis pertains to plan-and-execute model that essentially determines the nature of the target and the subsequent processing that needs to be followed. Radar can "see" objects – detected and located – at distances beyond the range of the human eye, and also with convenience and precision. Within the operable bounds or limitations on its performance, radar must detect the targets present in its range.

Passive channel processing in radar system is a method of determining the presence of a target and acts as a base for determining the nature of the target. In this study, we propose a method to perform processing on measurements obtained from a passive channel system. An algorithm is developed, which encompasses the elements of digital filtering and the desired output of the algorithm is a numerical value based on which the presence of a target is vetted. Further, the output value can act as a baseline for future computations.

At different stages during the work, certain limitations and real-time constraints were faced. All these limitations and constraints were suitably offset for and considerations to be made as a result of software simulators used were also accounted for. The results have been verified at each stage and also verified on a target board.

II METHODOLOGY

1Input Specification

The sampling frequency to be maintained throughout all components during model development is set at 160 MHz. We can observe data obtained for a total of 576 ms duration in 64 ms instants. The input has no specific form. Thus it can be continuous in nature or bursty. The approach is towards obtaining a bursty profile as noise measurements can be easily introduced.

A test input of 65,000 samples was taken for this study. This input is random and discrete signal with aperiodic variations. However at a later stage, there must be scope for the signal to be represented by a deterministic model. The input is as shown below.

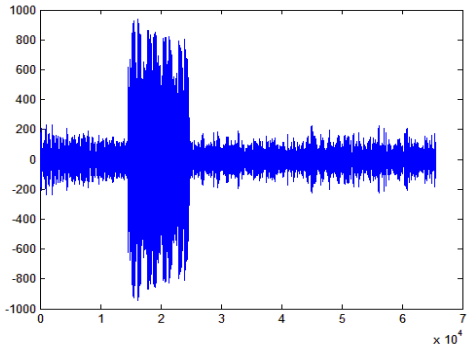

Figure 1. Test input spectrum

2 Proposed algorithm

The algorithm explained as follows lays down the basic framework based on which the processing of passive channel data is performed. In the absence of radar setup, suitable test input must be simulated using any of the available simulation platforms (MATLAB). The test input must then be brought to baseband level. This is mostly accomplished by multiplying the input samples with a local carrier and then passing them through a low pass filter. The frequency of this carrier is set at 60 MHz and the carrier can be either a sine wave or cosine wave. The low pass filter can be set to have a normalized pass band of 0.5 radians for the specified sampling frequency. At this point, the filtered samples need to be queued in a buffer, mainly to ensure that the burden on system memory is less and also to enable conversion to double datatype. Post this, filtering of the queued samples is done based on pre-defined conditions. At this stage, high pass filtering of the samples are performed at normalized pass band and stop

band instances based on the sampling frequency. The filtered samples must now be summed at enabled instances. The enabled instances are nothing but capturing the data at every 1 ms instant and adding them at the end of every 64 ms duration. The capture is done by means of activating an enable signal at the end of every 1 ms, and then performing summation after encountering 64 such enables.

At the end of each of these stages, the different outputs are observed and stored. Then, for physical verification of the model on a target board, the model must be ported to a hardware description language like VHDL or Verilog. Then after using a suitable methodology (either writing a top-down VHDL code or model implementation in Xilinx System Generator) the model must be synthesized and a programming file must be generated. This file is then downloaded onto FPGA board (field programmable gate array) and the respective signals must be tested for consistency inoutput.

3 Real-time constraints

There were a few real-time constraints faced during the simulation of the processing model. The major ones are touched upon here. Distinction of the exact filtering instant was an issue. This was sorted out only after comparing the values of samples before and after filtering. The main filtering function is also decided based on a set of specifications. This is essentially a trade-off between different aspects of functionality and the various design issues. Use of a high sampling frequency adds to an increase in the simulation time. Migration of the Simulink model into System Generator caused a few issues. The latter does not contain a buffer in its blocksets, which causes a significant increase in the already high simulation time.

III RESULTS

The figure below shows the output of the filtered baseband data. The input to this filter is the test input as shown in figure 1 multiplied with local carrier of 60 MHz frequency.

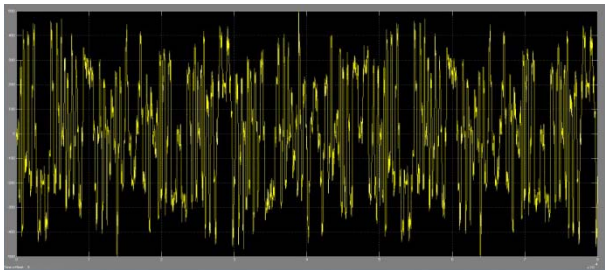

Figure 2 Filtered output from baseband data

The following figure shows the output frequency spectrum obtained after filtering and summation. The spectrum has a span of 160 MHz (sampling frequency) and is centered at 156.25 kHz.

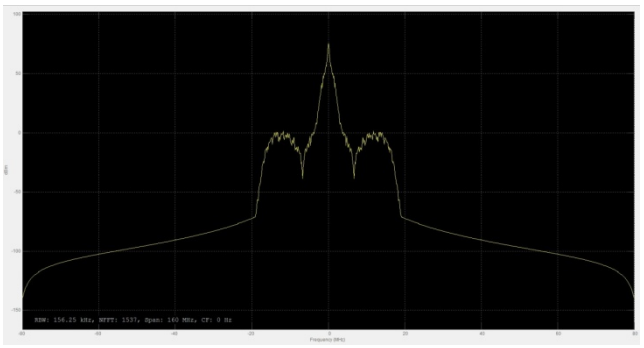

Figure 3 Output frequency spectrum

The next figure shows the workspace output post summation. This output is of the model developed in Xilinx System Generator. The subsequent figure (no. 5) shows the total output of the SysGen block.

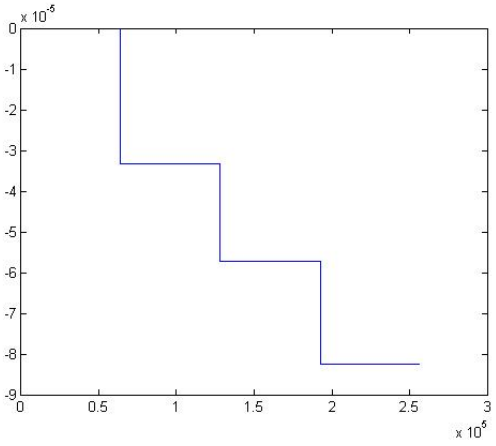

Figure 4 Sum output on workspace

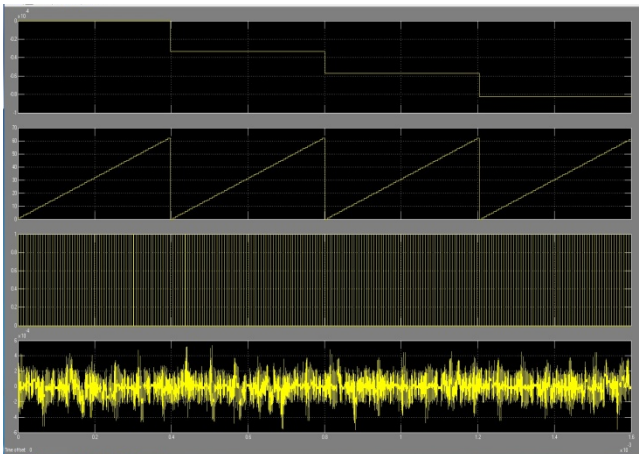

Figure 5 Total model output. a – Enable instantiated outputs, b – Count intervals, c – Generated enable signals, d – Sum output

The following figure is a plot of the result as verified by the FPGA board. Note that it checks for the output based on the enable signal. The enable signal is the trigger and only at instances when it goes high is the output observed.

The waveform was observed in Xilinx ChipScope Pro Analyzer. Xilinx Virtex – 6.

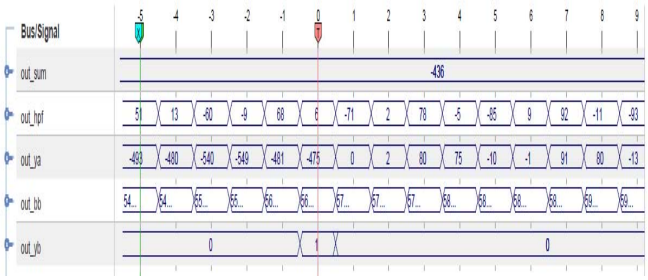

Figure 6 Output as verified on FPGA board

IV CONCLUSION

In this paper, an algorithm is proposed for effective and efficient processing of data as obtained from a passive channel system. Most of the analysis was conducted offline due to the lack of radar or sensing equipment. The nature of the work was mainly simulations on different programming platforms coupled with verification of the results on a target board. The results obtained were tallied with the results at different stages and the different limitations of the algorithm were also identified. The final results clearly show the detection of a target by the device and how on further processing, this information is conveyed to the end user of the data. As a future scope, a constant false alarm rate detector can be implemented in the algorithm and also detailed target statistics monitoring can be implemented in the algorithm.

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