Estimation of Pulse to Pulse Variations in the output of a Solid State Modulator Based 250kW C-Band Transmitter

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Abstract:

The paper describes the development of solid state modulator based 250 kW C-band transmitter meant for a Polarimetric Doppler Weather Radar. Testing and validating the transmitter's RF output stability is one of the key performance parameters in order to meet the required signal processing requirements. This is ascertained using pulse pair algorithm and the results obtained are presented.

Key Words: Solid State Modulator, Doppler, Pulse Pair Algorithm, Digital Receiver.

I INTRODUCTION

Doppler Weather Radar (DWR) is an important sensor for operations and research in the arena of atmospheric and meteorological sciences and is presently indispensable in the measurement and forecasting of atmospheric phenomena. DWR is globally used for forecasting storms, cyclones and other severe weather conditions, so that necessary preventive steps can be initiated to alleviate the impact of natural disasters on life and property. The Doppler Weather Radars deployed worldwide operate in 'S' and 'C' – band frequencies. A Dual Polarimetric Doppler Weather Radar, designed to operate in the C band has been developed by ISRO and Bharat Electronics Limited, and is the first of its kind in the country. 250 Kilo Watt Transmitter subsystem of this radar has been developed by Radar Development Area, ISTRAC, and the DWR is located in one of the ISRO Centers.

The Radar can be operated in volume scan or sector scan to collect the precipitation/rain data and is capable of detecting the echoes up to a range of 400km with a range resolution of 300m or better. The primary base products of C-band DWR are Reflectivity, Velocity and Spectrum Width. The measurement accuracy specification for reflectivity is 2dBz at 400Kms, for a rainfall equivalent of 23 dBz (1 mm/hr), at an antenna rotation of 2 rpm. Velocity and Spectral Width measurements have a targeted accuracy of 1 m/s at 250Kms, for a rainfall equivalent of 23dBz (1 mm/hr), at the antenna rotation of 2 rpm. The other base products are Differential Reflectivity and Differential Phase which make use of dual polarization. The accuracy requirement is specified at 0.25 dB at 250 Km for a rainfall equivalent of 12 mm/hr for the former and at 0.74 deg at 250 Km for a rainfall equivalent of 30 mm/hr for the latter, both at 2 rpm antenna rotation. These are summarized in Table-1.

PERFORMANCE SPECIFICATIONS		
SINGLE POL	Reflectivity	Velocity & Spectral Width
Range (Km)	*400*	*250*
Resolution (m)	*300*	*300*
Accuracy @ 23 dBz@ 2 RPM	*2 dB*	*1 m/s*
DUAL POL	Differential Reflectivity	Differential phase
Range (Km)	*250*	*150*
Resolution (m)	*300*	*300*
Accuracy	*0.25 dB*	*0.2 deg*

Table -1 Accuracy Requirements of C – Band DWR

In addition to these, there are more than fifty derived data products such as rain rate, rainfall accumulation etc, which are under research and constant improvement by scientists and meteorologists. Therefore, ensuring the coherency of the transmitter output sample is a pre-requisite for meeting the accuracy requirements of the DWR for its base products and the derived data products. Hence an investigation into the intra pulse and inter pulse variations is carried out using down-conversion and digitization techniques.

II C-BAND TRANSMITTER

The transmitter has a peak power of 250 kW and is capable of operating over a bandwidth of 50 MHz centered at 5.625 GHz. The signal for transmission is generated as a continuous wave at 5 dBm from a Coherent Signal Generator which has an OCXO stability of ±1ppb. An RF Driver Module then provides the requisite modulated RF Drive at 30dBm as input power to C-Band Klystron HPA VKC-8387K. The typical beam voltage and current required for a microwave output of 250kW as given in the data sheet of the klystron tube is - 44kV and 10A. The tube is cathode pulsed and the anode grounded. The cathode pulse is tuned at - 44 kV to meet the transmission power level of 250 kW and this is achieved using 5 IGBT based solid state modulator modules, each of which is rated for -4kV/80A along with a single 1:4 pulse transformer. The solid state modulator modules are charged in parallel from a -800V DC supply and they are

discharged in series in order to achieve a voltage of about -11 kV. This voltage pulse is applied at the primary of the 1:4 pulse transformer which makes the required cathode voltage available across its secondary.

III DESIGN USING TUBES

The conventional design of high power transmitters involves the use of High Voltage Power Supply (HVPS) to generate the cathode voltage required for the tube. Such a supply (eg. SPELLMANN make) is used to generate DC voltage of about -70 KV as in the case of 1Mega Watt transmitter developed by SAMEER, Mumbai and installed at S-band DWR; situated at one of the ISRO centers. The maximum current soured by the HVPS is in the range of 100 mA. A Tetrode is configured as a high power switch in order to switch the HVPS DC voltage according to the pulse width required for transmission. Such a design necessitates the development of a modulator card for swinging the grid voltage of the Tetrode. The screen grid voltage should remain constant even during the swing at the control grid and the modulator card remains floating at -70 kV. DC voltages for generating the swing at Control Grid and Screen Grid, along with several housekeeping power supplies have to be generated from 230VAC Line Input through a transformer. As the secondary of the transformer is getting connected to high voltage, very high insulation for secondary to primary (typically of the order of 100 kV) is necessary. Similar is the requirement if a Triode is used instead of a Tetrode, though the Screen Grid is not present. In either case, the modulator card would have to be floating at the cathode potential and therefore transformer grade oil insulation would be required for the card, its associated power supply sections and the bulky transformer. Maintenance of such a configuration is often cumbersome and a precise biasing of the Tetrode/Triode at such high kV is very tricky. Therefore, a modular approach using semiconductor devices is preferred for this application. Semiconductor devices are continuously replacing tubes in almost every arena, be it television, industrial, medical or transmitter applications. Hence, a modular -4kV/80A solid state modulator is designed and realized and a number of such modules are combined to achieve the required cathode voltage pulse.

IV A HYBRID TOPOLOGY

The IGBT based solid state modulator essentially functions like a pulsed high voltage power supply. This eliminates the high voltage DC supply (HVPS), the Tetrode/Triode switching circuit, the grid biasing cards, their isolated power supplies, bulky transformers and a huge energy storage capacitor used in earlier designs. Mainly the design of the solid state modulator is on Local Replaceable Units (LRU) based modular technology, which has a unique topology and is capable of providing high voltage pulse up to -20kV when connected in series.

A DC voltage of -800V is obtained from a -1kV high voltage rectifier. The rectifier has 3-phase 400V AC input through EMI line filters. 5 Nos of - 4kV/80A solid state modules are sourced by this -1kV DC Power Supply and are charged in parallel. With a rating of 6kVA, the output voltage of this supply is variable from 600VDC to 1000VDC. The solid state modules have IGBT as the switching elements in the charging and discharging paths. The IGBTs in the charging path are termed as 'Auxiliary IGBTs' and those in the discharging path are called 'Main IGBTS' and they get complementary trigger pulses. The storage capacitors connected across the -1kV section gets charged when auxiliary IGBT is triggered. During the pulse width of transmission the stored energy in the capacitor, gets discharged through the load, when Main IGBTs get triggered. All the modules are connected in parallel to main 1kV BUS for charging during 'OFF' periods of the pulse stream and they are connected in series with the klystron during the pulse width for transmission. Necessary high voltage isolation is provided by incorporation of suitable high voltage isolation diodes. Pulse widths up to 3.6μS and Pulse Repetition Frequency (PRF) from 100Hz to 1000Hz are supported using the present topology. The schematic of the 4kV/80A solid state modulator module is as shown in Figure-1.

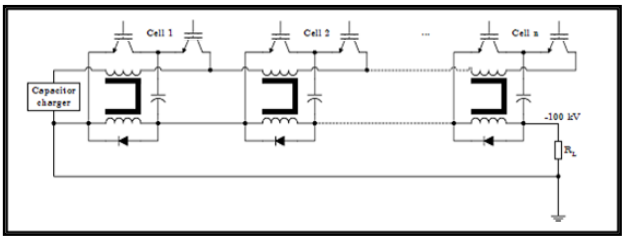


Figure-1 Solid state modulator topology

In the present case, a -11kV high voltage pulse from solid state modulators is applied to the primary of pulse transformer(PT) with 1:4 turns ratio for primary to secondary. The secondary of the PT is at -44kV which is connected to cathode of the klystron. The -1kV rectifier, solid state modulator modules and the trigger distribution module are co-located in the same rack. The Pulse Transformer and Klystron Filament transformer are housed inside the Klystron Tank in an adjacent rack.

V FPGA BASED TRIGGER DISTRIBUTION MODULE

An FPGA based trigger distribution module is used to synchronize the trigger pulses to the IGBTs such that they fire in unison in order to get the beam pulse with a narrow rise and fall time. IGBT devices have their own inherent turn on and turn off delays and the values may differ for different IGBTs of same part number. These inherent delays are to be compensated and all the IGBT pulse power supply cards are to be switched ON and switched OFF simultaneously with respect to a single TTL gate drive input. The TTL gate drive input is provided through fiber optic (F/O) link to the Trigger Distribution Module. An Actel FPGA duplicates this signal on 20 of its pins. The I/O buffers of the FPGA allow precise timing adjustment in order of few nanoseconds for these replicated signals. These electrical signals are converted into optical domain using fiber optic transceivers so that each Solid State modulator module card receives its respective gate drive through fiber optic (F/O) link. Here, the F/O link is chosen for providing HV isolation. By taking the input drive for a particular card as reference the timing of other channels are tuned for exact delay adjustment. With such architecture, a maximum beam duty of 0.04% and RF duty of 0.02% are achieved by

positioning the RF pulse within the flat top portion of the beam pulse.

VI PHASE VARIATIONS IN TRANSMITTER OUTPUT

Ensuring the coherency of the transmitter output sample is the pre-requisite for meeting the accuracy requirements of the DWR for its base products and the derived data products. The developments on the High Voltage switching side, using the topology mentioned in previous sections demanded an assessment of the stability of the transmitter RF output. Hence an investigation into the intra pulse and inter pulse variations is carried out using down-conversion and digitization techniques. This would ascertain the faithful amplification of the OCXO generated signal by the solid state driver amplifier and in turn by the Klystron Tube to 250 KW, apart from ensuring the stability of the solid state modulator subsystem.

VII MEASUREMENT SETUP

The Transmitter output sample at 5625 MHz is coupled through a Dual Directional Coupler. This output is attenuated by a high power attenuator to levels acceptable by a C-band mixer. The Local Oscillator port of the mixer is fed with 5595 MHz signal at a level sufficient enough to drive the diode mixer. The output at Intermediate Frequency port was fed through a Bessel Band Pass Filter with a bandwidth of 5 MHz centered at 30MHz. Bessel filters are chosen due to their property of constant group delay. The higher order products get filtered by the Band Pass Filter and its output is fed to a Digital Receiver sampling at 102 MSPS. Numerically Controlled Oscillator (NCO) frequency of the Digital Receiver is set at 30 MHz. The digital receiver derives all its internal clocks and frequencies from the externally supplied sampling clock. A pre-requisite step in the measurement is to phase lock the 5595 MHz Local Oscillator source and the Digital Receiver sampling clock source to the OCXO of the transmitter. The setup is shown in Figure-2.

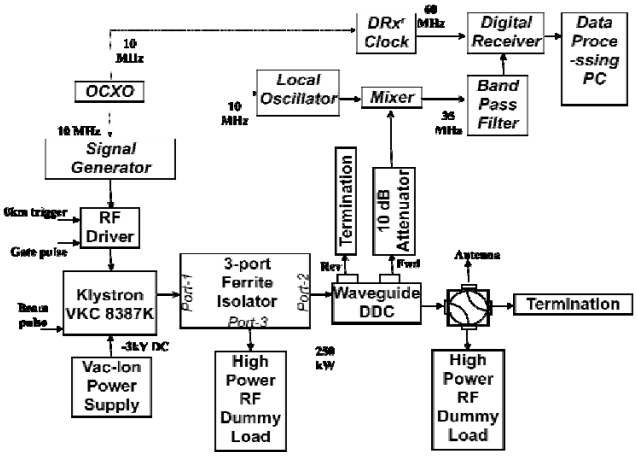


Figure-2 Integrated measurement setup

The digital receiver used is ECV4-2-2R105-XMC is a two-channel wideband digital receiver. The fundamental part of this receiver system is the Digital Down Conversion (DDC). Digital receivers often have fast ADCs delivering vast amounts of data; but in many cases, the signal of interest represents a small proportion of that bandwidth. A DDC allows the rest of that data to be discarded, allowing more intensive processing to be performed on the signal of interest. A direct digital down converter (DDC) typically performs channel access functions in all-digital receivers. The DDC Core accepts an input signal sampled at a high rate (~100 MHz), down converts a desired frequency band-of-interest (channel) to base band and adjusts the sample rate by a factor that is programmable. The DDC is typically located at the front-end of the signal processing conditioning chain, close to the A/D, and is usually required to support high-sample rate processing in the region of 100+ mega samples per second.

In the present case, the ECV4-2-2R105-XMC digital receiver combines two channels of high speed A/D conversion with high end Virtex-4 FX100 FPGA, along with 256 Mbytes of DDR SDRAM and 2 Mbytes Dual port SRAM. One Xilinx Virtex- 4 FPGA functions as the primary data processor. This FPGA allows the user to run custom algorithms such as digital down/up conversion (wideband or narrow-band), Fast Fourier transforms (FFT), and filtering directly on the board. The second Virtex-4 FPGA is dedicated to the PCI/PCI-X interface. The digital receiver is available as a single XMC board and was mounted on a Mercury VPA-200 Dual 7448 VXS Single-Board Computer (SBC) for the measurement. The SBC was housed inside a Schroff VXS/VME64x Tower System and was programmed using a Real Time Operating System (VxWorks) platform. These are shown in Figure -3.

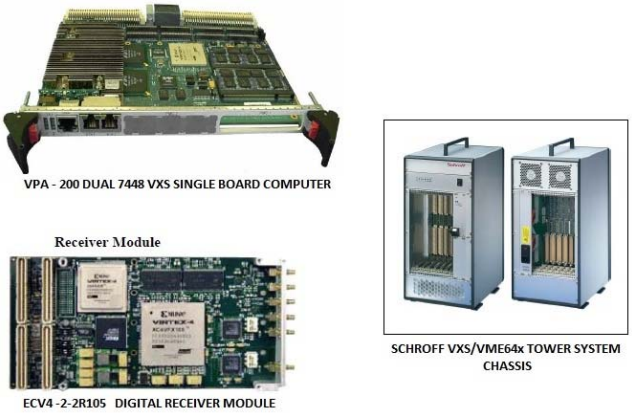


Figure-3 Digital Receiver Hardware

The A/D of the input channel is designed around the Analog Devices AD6645-105, with a maximum sampling rate of 105 MSPS and has 14 bit resolution. Multi-tone Spurious Free Dynamic Range of 100 dB and I/F sampling to 200 MHz are its key specifications. The numerical controlled oscillator is 32 bit and a 5th order CIC filter and a decimating FIR filter are present for decimating the data by a factor of 2 to 16.

VIII PULSE PAIR ALGORITHM IMPLEMENTATION

Pulse-Pairing provides an estimate of the changes occurring in the amplitude and frequency of the transmitter output sample by determining the average phase shift and amplitude shift that has occurred from PRF to PRF, averaged over several PRF. More number of PRF equates

to less noise, giving more accurate estimates. I&Q data samples describe a complex vector that will rotate at a speed directly related to the frequency variations in the signal. The i^{th} sample is represented as:

$$S[i] = I + jQ$$

An Auto-Correlation algorithm is applied to each individual range bin, across several PRF, and is defined as below:

$$\text{Lag}[n] = \sum_{i=0}^{N-1} (\tilde{S}[i] * S[i+n])$$

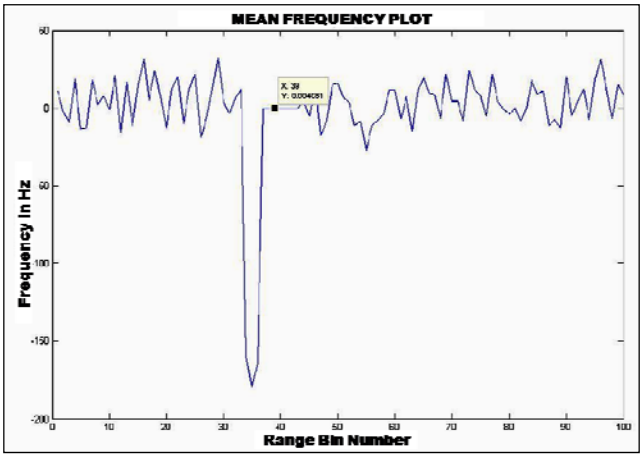
Where N is the number of PRF samples and $\tilde{S}[i]$ is the conjugate of S[i].

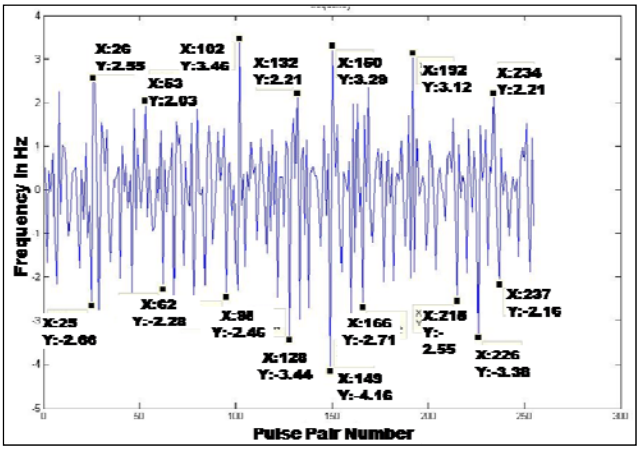
The real component of lag [0] provides Intensity information and the phase of lag [1] provides Doppler information. In the present case, the decimation value of the digital receiver is set to one and the first 100 range bins are acquired for each Pulse Repetition Interval.256 such PRTs are acquired. The Processing algorithm is implemented on MATLAB. Firstly, the residual error in the down conversion and the digital receiver is ascertained. This is done by feeding pulsed RF signal at 5625 MHz along with simulated doppler values into the mixer. Such an exercise helps in characterizing the measurement chain comprising of C-band Mixer, Band Pass Filter, Local Oscillator, Digital Receiver and the Processing Algorithm. In the actual measurement with the transmitter output sample, the measured values are within an error of +/- this residual error value. As shown Table -2, the accuracy with the measurement set up has been estimated to be in the order of +/- 1 Hz by such a method.

SNo	Simulated Doppler(in Hz)	Max Variation(Hz)
1	1	1.816 to -0.02
2	10	10.94 to 9.08
3	20	21.07 to 19.15
4	30	30.90 to 29.00
5	40	40.96 to 39.02

Table -2 Accuracy of Measurement

The Transmitter output sample (5625 MHz) at the coupled port (+14 dBm) after a 1:2 power diver was fed to a mixer after attenuation by 10 dB. The transmitter was operated at 1 KHz PRF and 1 us Pulse width. The power level at the input to the mixer was around -12 dBm [power divider loss: 3.3 dB, cable loss: 6.7 dB, external attenuator value: 10 dB]. The LO port of mixer was fed with 5595 MHz CW signal at 2 dBm level. The output at IF port after band pass filtering was measured to be around 220mV at 30MHz. This was fed to Digital Receiver, sampling at 102 MSPS (0dBm clock level) with NCO frequency set at 30 MHz. The decimation value is set to 1 and 256 PRTS are acquired, with 100 range bins each. Pulse Pair Algorithm is used to measure the frequency shift in each pulse. As the transmitter pulse is delayed w.r.t the trigger for DRx, it is detected at the 39^{th} range bin as shown in Figure – 4 (a). It is to be noted that Figure 4(a) shows the average value for 39^{th} range bin for 255 pulse pairs. The variation within 255 Pulse Pairs for this range biun is shown in Figure – 4 (b). Instead of averaging all the 255 pulse pairs, 20 pairs are averaged, which is more close to the real scenario. 12 sets of values are so obtained and the values for six such acquisitions are summarized in Figure – 4 (c). The signal processing algorithm using pulse pair technique is implemented on MATLAB.





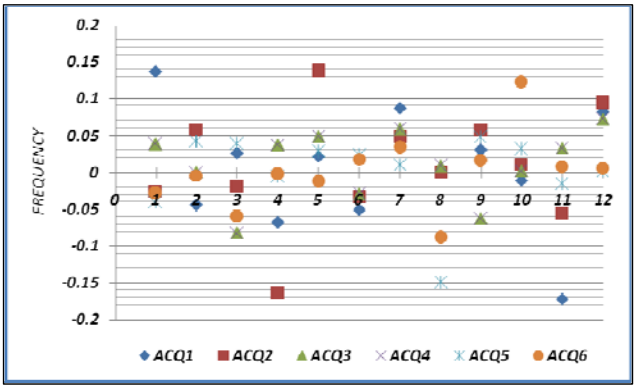


Figure – 4(a) Averaged value for 256 PRTs, 4(b) Variation across 255 Pulse Pairs 4(c) Averaged value for sets of 20 PRTs for 6 acquisitions

The Experiment is repeated with simulated Dopplers of 1, 10, 40,400 Hz values in order to ascertain the performance as in actual operation. The Doppler shift is made at the RF generation point itself in the OCXO based signal generator. The worst case deviation of the detected Doppler frequency with the simulated Doppler frequency is about +/- 4 Hz. Similar is the observation with Transmitter sample (without Doppler). However, it is to be noted that the above readings are with a measurement accuracy of +/- 1 Hz as brought out in residual error measurements by feeding simulated Doppler frequencies (Table -2). The average deviation of the detected Doppler

from the simulated Doppler for 20 pulses averaging is +/- 0.05 Hz only. This ascertains the faithful amplification of the RF signal by the solid state driver amplifier and in turn by the Klystron Tube. It also certifies the stability of operation of the modulator circuit at the rated voltage for the tube. The results are shown in Figure 5.

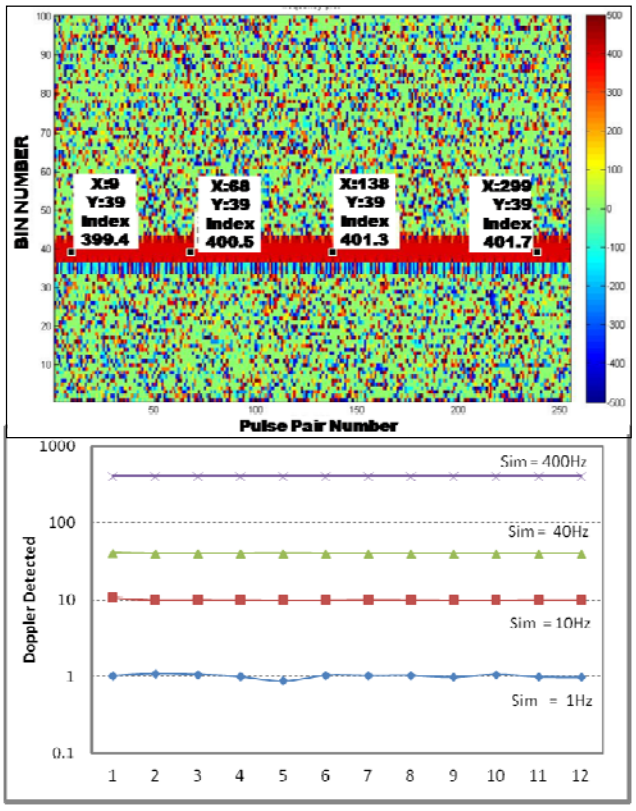


Figure 5(a) Simulated Doppler of 400 Hz detected 5(b) Doppler detection for various values, with averaged value for sets of 20 PRTs for 6 acquisitions

IX CONCLUSION

The worst case deviation of the detected Doppler frequency with the simulated Doppler frequency is about +/- 4 Hz with a measurement accuracy of +/- 1 The average deviation of the detected Doppler from the simulated Doppler for 20 pulses averaging is +/- 0.05 Hz only. The investigation into the pulse to pulse variations of the transmitter output has shown that its is very much possible to achieve the performance specifications for the C – Band DWR in terms of the accuracy requirements for the base products and several derived data products. The coherency of transmission and stability of the transmitter subsystem is therefore ascertained.

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