# Digital Beam Steering and Timing Controller for X-Band Phased Array Radar


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**Abstract—** The Objective of this paper is to design an FPGA based beam steering controller for active phased array radar. The Beam steering controller basically receives the beam direction information from the radar computer and computes the phase control values for each of the TRMs (Transmit Receive Modules) of the antenna array.

Active phased array radar consists of an array of antennas in which the relative phases of respective signals feeding the antenna are varied such that the effective radiation pattern of the array is reinforced in a desired direction. It consists of amplifiers or processors in each phase shifter element.

The Beam steering controller plays a vital role in steering the antenna beam of active phased array radars where beams are formed electronically. The Transmit / Receive Modules (T/R Modules) are key parts of advanced phased array radar systems. In order to produce beam pattern from multiple radiating elements, the phase angle of each T/R Module must be assigned with a calculated value. When Common phase gradients are sent to all Transmit / Receive Unit Controllers (TRUCs), the respective phase values are calculated for the radiating element associated with them. The calculation of optimized 6-bit phase angle from the phase gradients carried out using FPGA. The implementation was carried out using the Xilinx Virtex 5.


## I. Introduction

Electronically steered array antennas (ESAA) are now employed in many latest types of radars. With the advent of aircraft designed with an extremely low radar cross section the pressing need for excellent beam control and frequency agility has become a necessity in recent years. Therefore, avionics designers have given the ESAA more attention than any of the other advanced radar concepts.

Beam steering in this regard involves changing the direction of the main lobe of a radiation pattern. Steering was originally achieved by mechanically rotating the antenna. A more advantageous method is to electronically steer the beam and which is employed in the ESA and subsequently in the phased array radar. There are two types of ESA's

1. Passive ESA
2. Active ESA

Active phased array antennas are used in this work. A phased array is a directive antenna made up of a number of individual radiating elements that have a progressive phase shift. The beam can be electronically steered by changing the phase and power of the current at each element. The phase shift that is given to and power to be radiated by each element is controlled by the Beam Steering Unit (BSU). The beam of a large fixed phased-array antenna therefore can be rapidly steered from one direction to another without the need for mechanically positioning a large and heavy antenna.

## II. Functional Block Diagram

The functional diagram which forms the basis of this project is shown below. The functional diagram of the distributed beam steering unit shows the data/signal flow from PC to radiating elements with the different interfaces.

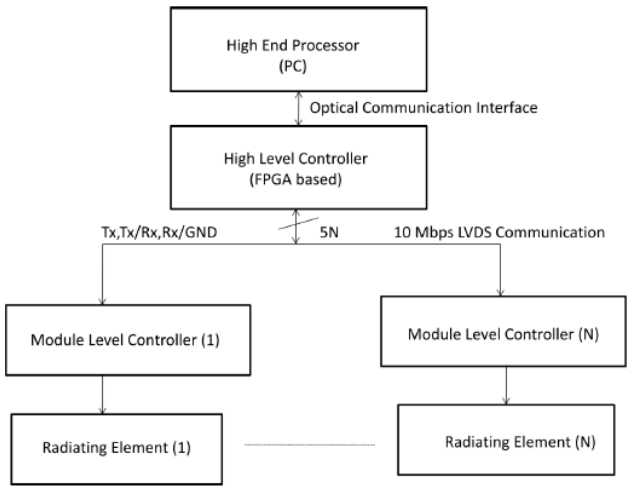



Fig 1:Functional Block Diagram of Phased Array Radar

An electronically scanned phased array antenna system comprises a phase shift controller corresponding to each antenna array element for individually computing a phase shift value which governs the phase of the signal associated with the corresponding antenna element. The computed phase shift values of all the phase shift controllers affect the signals of the antenna elements to point the antenna beam in a specified direction. Each of the phase shift controllers is programmed with a predetermined incremental phase shift

value for computing a sequence of phase shift values at specified intervals. This sequence of phase values computed for the elements of the phased array cause the antenna beam to be scanned in a corresponding direction. The beam can thus easily be switched from one direction to another by computing and feeding new phase values to the phase shifters.

In the hardware implementation , since the BSU sends phase values to the phase shifters in all transmit/receive modules and needs to receive the information about status of the beam, the Beam Steering Unit establishes communication between Graphical User Interface (GUI) and the transmit/receive unit controllers.

Description of the Functional Block Diagram

1. High End Processor

The high end processor calculates the phase gradients from the azimuth and elevation angles given as input and sends those values to the high level controller (FPGA based). A separate GUI may be provided for calculation of the phase gradients. This communication takes place over an optical interface.

2. High Level Controller

The high level controller is located between the processor and the module level controllers. It distributes commands received from processor to the transmit/receive modules. It also receives status reports from the module level controllers and again transmits them back to the processor. The communication between them is through a pair of Low Voltage Differential Signaling protocol. The baud rate for this communication is 10 Mega bit per second. Field Programmable Gate Array is used for the realization of this controller because of the following reasons:

- Ideal for customized design
- Offer the advantage of high integration
- Avoid the problem of ASIC□s like high cost and increased delay

output should not normally exceed the threshold if noise plus clutter alone were present, but the output would exceed the threshold if a strong target echo signal were present. If the threshold level were set too low, the unwanted signal might exceed it and be mistaken for a target [9]. This is called false alarm. If the threshold were set too high, unwanted signal might not be large enough to cause false alarms, but weak target echoes might not exceed the threshold and would not be detected. When this occurs, it is called a missed detection.

3. Module Level Controller

These are the units which control the transmit/receive modules. They receive the commands from the high level controller. These controllers decode the message received from the upper levels, convert them into digital data in the form of bits and feed the appropriate values to the phase shifters and the attenuators that are connected to the transmit/receive modules. They also collect information about the beam status and the proper working of the modules and send to the high level controller. Since this is a distributed Beam Steering Unit, every module has a separate controller associated with it.

4. Radiating Elements

The radiating elements are the actual antenna elements of the array. The phase shifts given to the phase shifters and the amplitude control data are ultimately used to act upon these radiating elements so that the beam-forming beam steering is practically achieved.

## III. Logic Flow Diagram

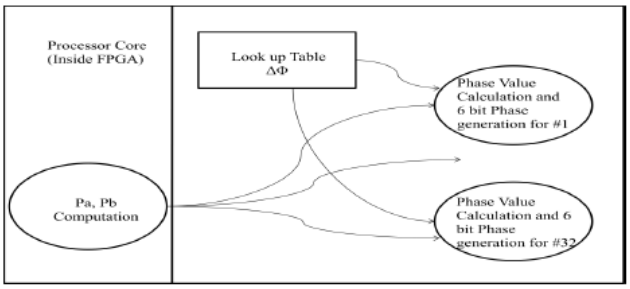



Fig 2: Logical Implementation of ABCU Unit

Steps Involved in Logic Flow:

1. Reception of dwell information from RC (BSU or ABCU receives azimuth and elevation Direction information from RC).
2. Phase gradient Computation (PRT Wise) from initial beam direction.
3. Phase value calculation with error for 32 TRMs.
4. 6 bit phase control generation for 32 TRMs.

| Normal 6 bit phase ctrl generation | FPGA resource and time saving logic for 6-bit phase ctrl generation |
|---|---|
| $Pa= (2\pi/\lambda).dx.\sin\Phi.\cos\theta$ | $Pa= (2\pi/\lambda).dx.\sin\Phi.\cos\theta$ |
| $Pb = (2\pi/\lambda). dy'.\sin\theta$ | $Pb = (2\pi/\lambda). dy'.\sin\theta$ |
| $\Phi_{ct} = m . Pa + n . Pb + \Delta\Phi$ | $\Phi_{ct} = m . Pa + n . Pb + \Delta\Phi$ |
| $ctr1= \Phi_{ct}/5.625$ | $ctr1= \Phi_{ct}/64$ (Truncation of last 6 bits) |
| Ctrl2=round(ctrl1) | Ctrl_final=ctrl1+Ctrl_error |
| Ctrl_final=ctrl2+Ctrl_error | |

Table 1: Formulas Used for Calculations.

## IV. Implementation of Beam Steering Unit

The Beam steering controller plays a vital role in steering the antenna beam of active phased array radars where beams are formed electronically. The Transmit / Receive Modules (T/R Modules) are key parts of advanced phased array radar systems. In order to produce beam pattern from multiple radiating elements, the phase angle of each T/R Module must be assigned with a calculated value. The implementation of BSU is as shown in figure 3.

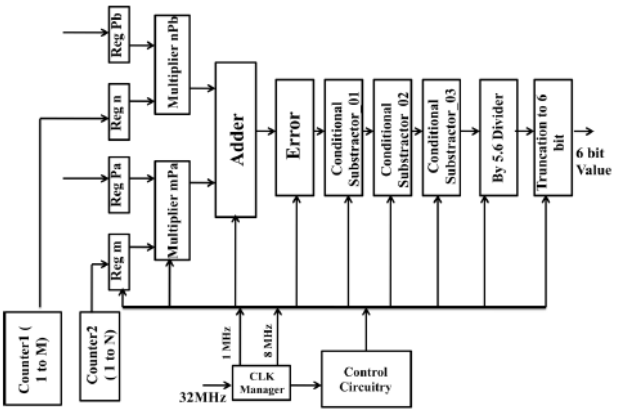



Fig 3: BSU implementation block diagram

When Common phase gradients are sent to all Transmit / Receive Unit Controllers (TRUCs), the respective phase values are calculated for the radiating element associated with them. The position of a T/R Module in the array decides the phase angle of corresponding radiating element. The calculation of optimized 6-bit phase angle from the phase gradients carried out using FPGA.

A. Calculation of 6 bit phase controlled value

The scan-to-scan discriminator uses one of the three approaches mentioned below in order to distinguish between the marine the targets and the unwanted signals.

The inputs to the receiver (signal processing unit) are the three signals that are produced by the antenna- the azimuth, elevation angle and frequency. The phase gradients are calculated with the azimuth and elevation angles of the beam to be steered. The two phase gradients are calculated as follows by the following formulae.

$$Pa=2\pi/\lambda * dx * \sin(az) * \cos(el) \quad (1)$$

$$P_b=2\pi/\lambda * dy * \sin(el) \quad (2)$$

$$\Phi_{ct} = m . Pa + n . Pb + \Delta\Phi \quad (3)$$

$$\text{6 bit phase control} = \Phi_{ct}/ 5.625 \quad (4)$$

Where az- Azimuth angle

el- Elevation angle

dx- Distance between two radiating elements in horizontal direction

dy- Distance between two radiating elements in vertical direction

λ- Wavelength.

Here Pa is calculated for azimuth and elevation positions and Pb is calculated for elevation position and vary from -180º to +180º. The phase gradients are calculated as decimal values and later converted to binary values. The phase gradients can be represented with 8 bits. In order to follow the uniformity among all the phase gradient values, all the phase gradient values are represented with 8 bits.

The algorithm for calculation of 6-bit phase value from phase gradients is as follows:

Step 1: Receive the phase gradients in synchronous serial link.

Step 2: Obtain individual products m*Pa and n*Pb.

Step 3:Obtain the phase product resulting from the calculation

$$\Phi ct = m . Pa + n . Pb + \Delta\Phi$$

The obtained phase product is of 8bits.

Step 4: Divide the Phase product by 5.625(rounding to 6) using pipelined Divider logic core and store the reminder. Obtained remainder is 6bits.

**Flow Chart for BSU Implementation is Shown in figure Below**

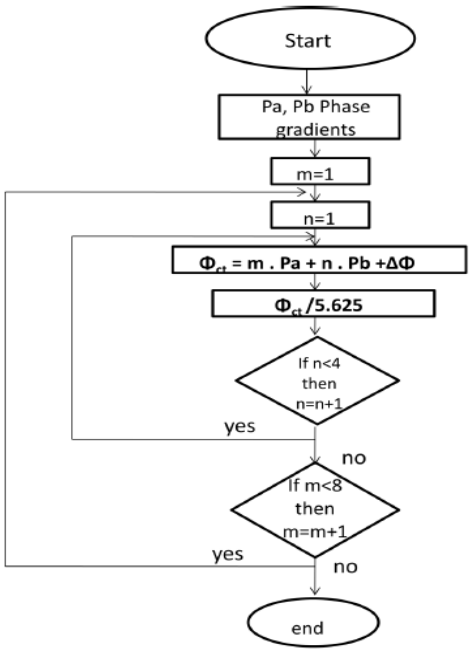



Fig 4: Flow Chart

## V. APPLICATION

The BSU is a very important unit in electronically steered phased array. Some of the applications are listed as follows:

- Multiple angles and/or multiple point inspection from a single point – the modern BSU allows the physical antenna to be kept stationary and only the beam will be switched from one direction to another.
- Easy detection and correction of Phase errors – the values provided to the phase shifters can be compared with the lookup tables to detect and rectify them.
- Accurate beam steering and low side lobe level realization – using the different amplitude distributions like Taylor, Chebyshev, Kaiser etc., suitable weights can be applied to the array elements to achieve the side lobe level reduction.

## VI. RESULTS AND DISCUSSIONS

**MATLAB Simulation Results:**

A. The simulation result for array factor of linear array is shown in the Figure 5. The following observations can be made:

- The main lobe of the beam is at zero degrees since there is no steering applied to the beam.
- It consists of side lobes, Since no side lobe reduction techniques are used.
- This graph has been plotted with f=9.5 GHz.
- The y-axis is magnitude in dB and x-axis is theta in degrees.

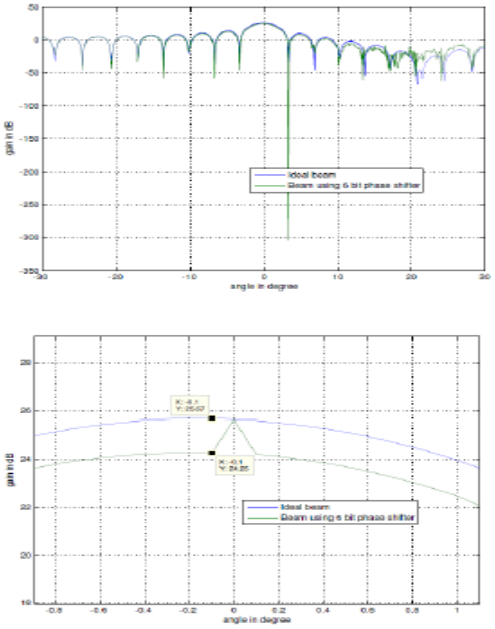



Fig 5: Beam Pattern at 0deg.

B. The simulation result for array factor of rectangular array is shown in the Figure 6. The following observations can be made:

- The main lobe of the beam is at -5 degrees since steering applied to the beam.
- The side lobe levels (SLL) are high, since no side lobe level reduction techniques are used.
- This graph has been plotted with f=9.5 GHz, n=4, m=8.
- The y-axis is magnitude in dB and x-axis is theta in degrees.

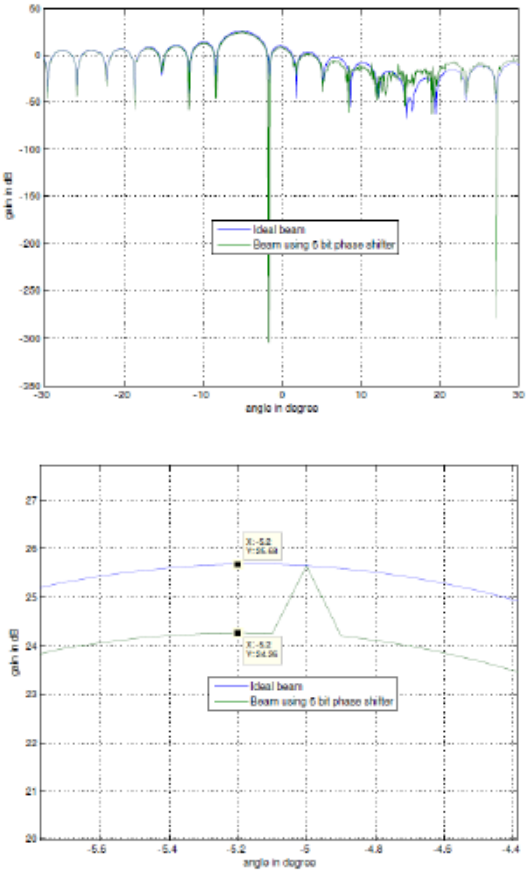



Fig 6: Beam Pattern at -5deg

C. The simulation result for array factor of rectangular array is shown in the Figure 7. The following observations can be made:

- The main lobe of the beam is at +5 degrees since steering applied to the beam.
- The side lobe levels (SLL) are high, since no side lobe level reduction techniques are used.

- This graph has been plotted with f=9.5 GHz, n=4, m=8.
- The y-axis is magnitude in dB and x-axis is theta in degrees.

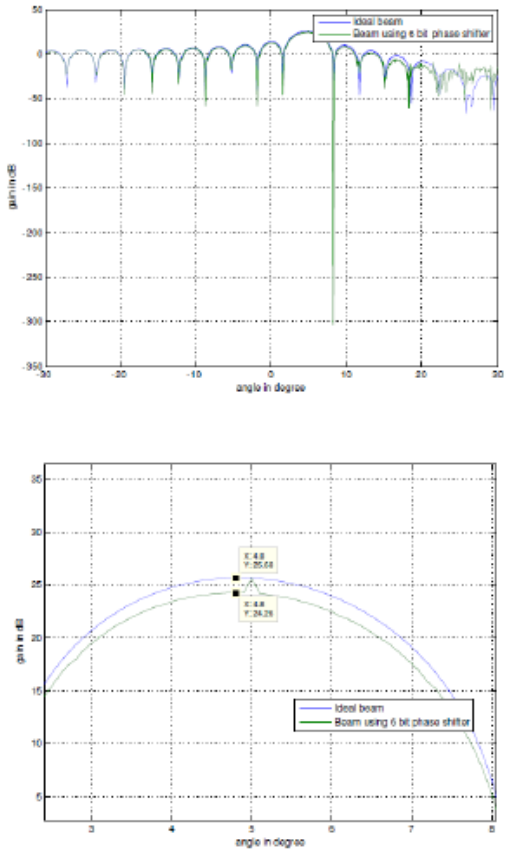



Fig 7: Beam Pattern at +5deg.

D. The simulation result for array factor of rectangular array is shown in the Figure 8. The following observations can be made:

- The main lobe of the beam is at -10 degrees since steering applied to the beam.
- The side lobe levels (SLL) are high, since no side lobe level reduction techniques are used.
- This graph has been plotted with f=9.5 GHz, n=4, m=8.
- The y-axis is magnitude in dB and x-axis is theta in degrees.

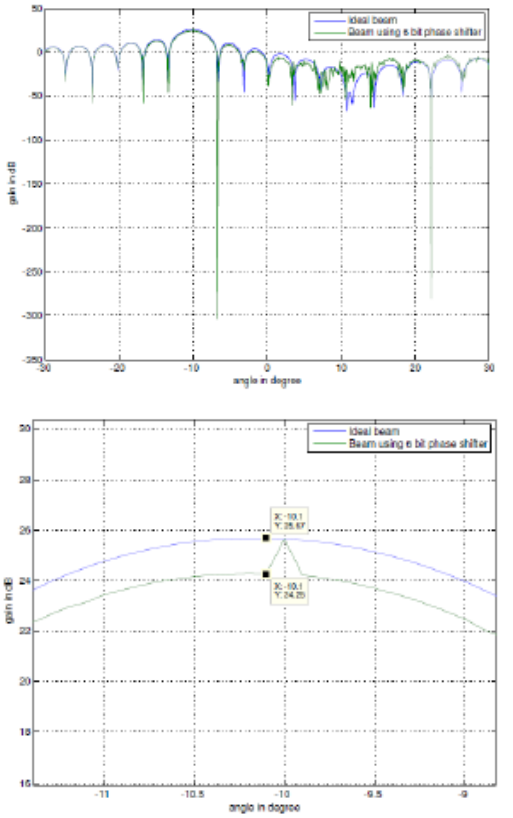



Fig 8: Beam Pattern at -10deg.

E. The simulation result for array factor of rectangular array is shown in the Figure 9. The following observations can be made:

- The main lobe of the beam is at +10 degrees since steering applied to the beam.
- The side lobe levels (SLL) are high, since no side lobe level reduction techniques are used.
- This graph has been plotted with f=9.5 GHz, n=4, m=8.
- The y-axis is magnitude in dB and x-axis is theta in degrees.

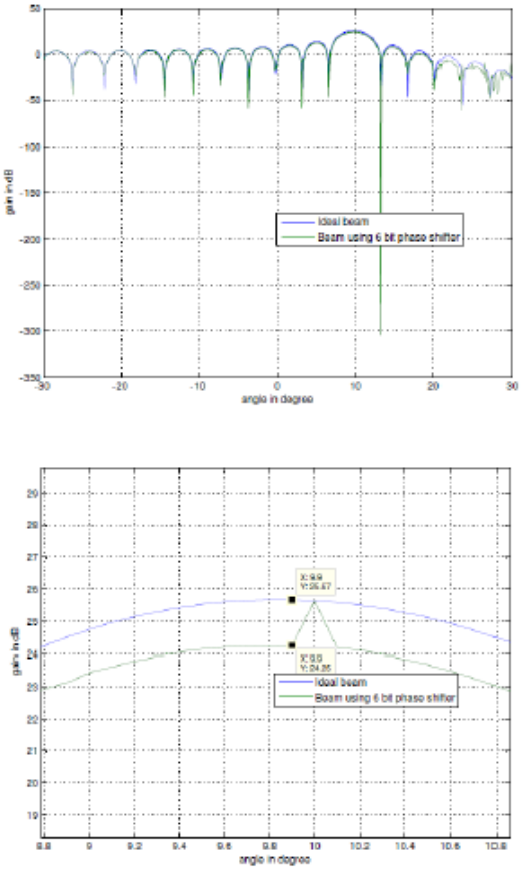
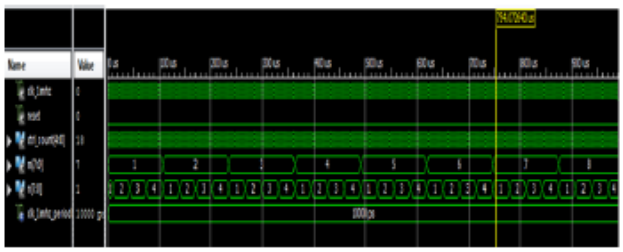



Fig 9: Beam Pattern at +10deg.

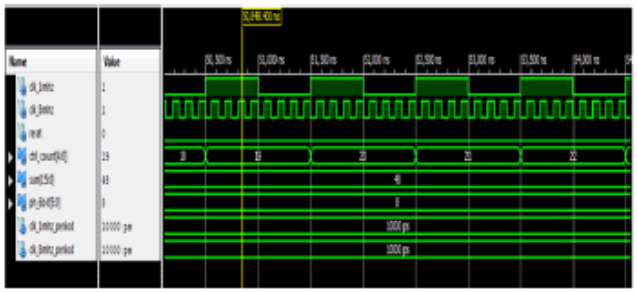
**Xilinx ISE Simulation Results**

A. Schematic waveforms before adding error

The control counter is varied from 00001 to 11111. In the figure below, when ctrl count is 00001, the values of m and n are taken as input which varies from 1 to 32 elements. The value of Clk = 1MHz and Reset=0.



When Clk_count=00010 products m*pa and n*pb is calculated, using input Pa=15, Pb=16,m=5,n=4. When Clk_count=00011 sum= m*pa+n*pb is calculated, when Clk_count=00100 to 01001 the sum value is continuously subtracted by 360 till the sum value is less than 360. When Clk_count=01010 , clk_1=1MHz, clk_2=8MHz,reset=0 phase value is converted to 6bit by dividing phase value sum by 6 (round of 5.625). Figure below shows the VHDL output in schematic waveform.



The simulated result for input Pa=15, Pb=16, m= 1, 2, 3, 4, 5, 6, 7, 8,n=1, 2, 3, 4,reset=0. The phase value is computed using the equation Φct= m*Pa + n*Pb . Then the ph_6bit_out (6 bit output) is calculated for all 32 values by dividing all values by 5.6. The reset used here is an active low signal as shown in figure below.

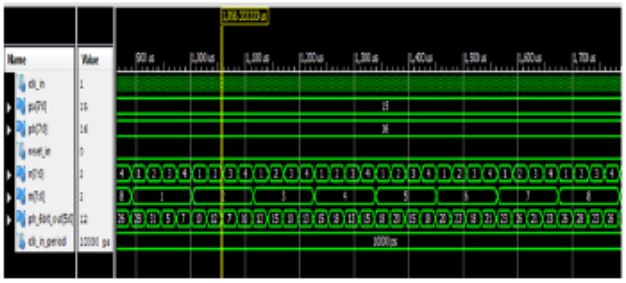
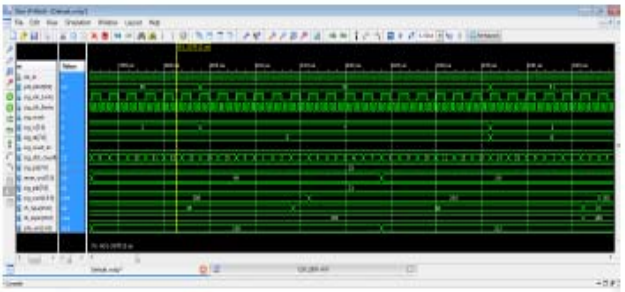
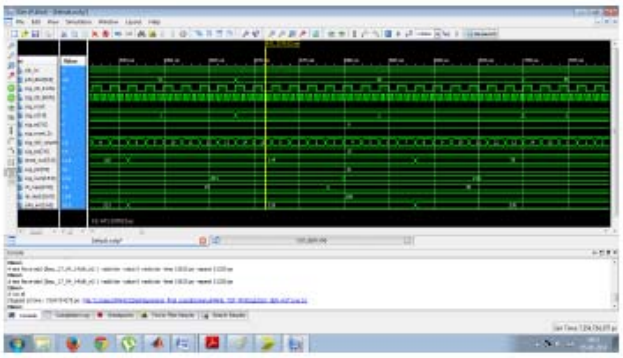


Fig 10: VHDL output before adding error.

B. Schematic waveforms after adding error

The simulated result for input Pa=16, Pb=32, m= 1, 2, 3, 4, 5, 6, 7, 8,n=1, 2, 3, 4,reset=0. The phase value is computed using the equation Φct = m . Pa + n . Pb + ΔΦ . Then the ph_6bit_out (6 bit output) is calculated for all 32 values by dividing all values by 5.6. The reset used here is an active low signal as shown in figure below.







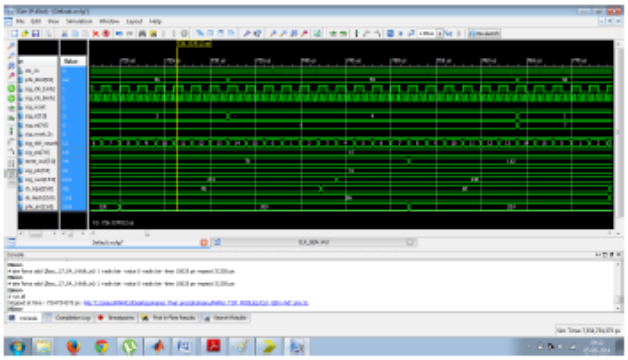


Fig 11: VHDL output after adding error.

**Chip Scope Simulation Results**

**A.** Chip Scope waveforms before adding error

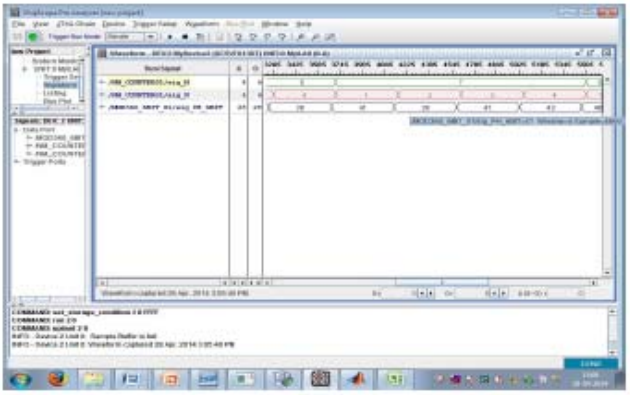


Fig 12: Chip Scope Output waveform before adding error.

B. **Chip Scope waveforms after adding error**

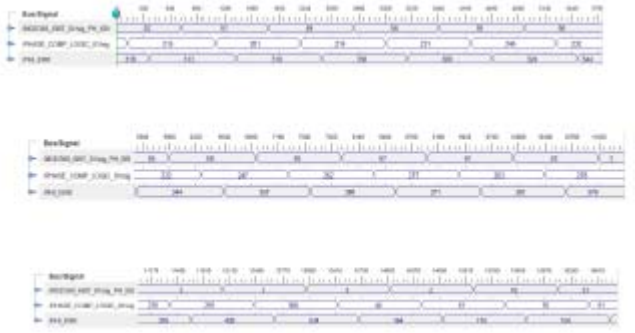


Fig 13: Chip Scope Output waveform after adding error.

## VII. CONCLUSION AND FUTURE SCOPE

It is concluded that 6 bit phase value was calculated and assigned for each of the Transmit/receive modules of phased array antenna in order to steer the beam in particular direction. The 6 bit phase shifter can be replaced by 7 or 8 bit phase shifters to improve the precision. It is also concluded that beam steering unit is realized by using VIRTEX5-XC5VFX130T-1FF1738C FPGA board. The functional interface and timing requirements as per specification are achieved.

The radiating elements can be extended to larger arrays like 64, 128, 256, 512, 1024 etc thus side lobes can be reduced considerably.

- The error obtained during the calculation of phase value and actual phase value can be minimized.
- Side lobe reduction technique can be added.
- It can be enhanced to Octal Transmitter/ Receiver module controller (OTRMC), which is capable of controlling 8 Transmitter/ Receiver modules.
- Use of division algorithms like “non restoring division algorithm” instead of IP cores will allow the design to be implemented on FPGAs other than Xilinx such as ACTEL FPGAs.

## VIII. REFERENCES

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**Author Index**

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**Shri. V. Mahadevan** obtained his B.Tech (Hons) in Electronics & Communication from IIT Kharagpur and M.E. in Communication Engineering from IISc Bangalore. He joined ISRO Satellite Centre in the Communication Systems Group and contributed in the design and development of Antenna & Passive Systems flown in all the spacecrafts. One of the major contribution is in the development of Active Phased Array Antennas which was successfully flown and is being adopted for many future spacecrafts. He was appointed as Associated Project Director for CATF ( Compact Antenna Test Facility) and the same was established in ISRO Bangalore in a record time. He held a number of posts in various satellite projects and finally appointed to the post of **Group Director, Communication Systems Group,** ISRO Satellite Centre, Bangalore. He retired on superannuation in April 2010 and is presently serving as Professor in the Dept. of Telecommunications at PESIT ( An autonomous Engineering College under VTU and UGC Delhi), Bangalore.

He received NRDC award from Govt. of India for his contribution on **Handheld Antenna for Satellite Telephone**, Team Award For **Cartosat-2 Satellite** from President of India, ISRO Award for **Phased Array Antenna System**, and **IRSI-IETE 2007** Award for Contributions on **Spacecraft Omni directional and Phased Array Antenna System**. He holds two **Patents**, one Handheld Antenna System and the other on UltraLow Sidelobe Antenna. He is a Senior Member of **IEEE**, Life Member **ASI** (Astronautical Society of India) and Life Fellow Member **IETE, M**ember **IET** and has published a number of papers in international and national journals.

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