High Power GaN based L-Band TR Module

Swaraj Varshney[1], Rajashekhar chowhan[1], Chandan Kumar[2], Somsing Rathod[1]
Benoy Kuriakose[1], K Sreenivasulu[1]
[1]Electronics and Radar Development Establishment (LRDE)
[2]Defence Avionics Research Establishment (DARE)
C.V. Raman Nagar, Bangalore– 560093, INDIA
swaraj.varshney@lrde.drdo.in

Abstract:

Transmit / Receive Module (TRM) plays a vital role in deciding the performance of any Active Antenna Aperture of Radar. Continuous improvement in the architecture and design strategies of different components of T/R Module is taking place all over the world. A lot of research has been invested in increasing the Transmit output power of TRM along with improved efficiency keeping the physical form factor same. The key design constraints in designing TRMs especially for Radar are its Tx Output power, Module Efficiency, Rx Gain along with its Rejection , Rx Noise figure (NF), DC Supply and most importantly the form factor and weight . Often achieving these specifications all at once is quite challenging in TRM design. On one side, Tx Output power and NF decides the maximum range of Radar; other side efficiency of TRM dictates the cooling load of the Radar. Even weight and form factor have a bigger role to play as TRMs are used in number in a active antenna array configuration. One such multi constraint narrowband GaN based DTRM (Dual TRM) design is attempted for military L-Band with about 15% bandwidth and developed successfully. Gallium Nitride (GaN), being wide band gap material, offers appealing features like High Power and better efficiency when compared to other contemporary process technologies. The developed DTRM has a Output power of min. 200W peak in Transmit for each channel and Noise Figure of 3.5 dB max with Band Pass Filter before LNA in each receive chain. It occupies an approximate size 230 mm× 90mm×35mm . Complete TRM needs a single +50V supply and offers minimum 35% efficiency.

TRM is also designed to provide the Phase Shift and Attenuation in Transmit or Receive mode controlled by the System. It protects its receiver part against High Level Return Power (from the antenna). Moreover, it gives information about its functionally state to the system using FPGA Control Card. Besides, It has got a power conditioning card which generates the DC supply voltages to the various devices and circuits

Key Words: ***T/R Module, Transmit Chain, Gallium Nitride, L-Band, High Electron Mobility Transistors, HEMT, Heterojunction Bipolar Transistor, ADS, Power Amplifiers, Active Phased Array Radars.***

I. INTRODUCTION

Active Electronically Scanned Array (AESA) has evolved to the extent that all future radars would employ this technology into a variety of systems and platforms having broad mission areas of Air Defense, Ground and Sea surveillance. T/R-modules are the key elements in the active phased array antennas for radar and electronic warfare applications.

The driving force for the development of the next generation T/R-module is no longer performance alone. As AESA frontends consist of hundreds, thousands, or even ten thousands of elements per aperture, the T/R-module has a big impact on size , cost and weight of the entire antenna.Today the main trend for performance improvement both in transmit and receive operation is the application of the GaN technology. With this new semiconductor technology T/R-modules with higher transmit output power and higher efficiency is feasible even in smaller form factor.

In this paper of L-Band TRM design, current state-of-the-art GaN technology has been implemented for Transmit chain in order to develop small size dual channel 200W Output power T/R Module for military Band over 200MHz Bandwidth. It briefly touches upon various design aspects like Power budgeting, Device selection, Bias and Stability of the circuits and impedance matching for the power amplifiers. Required simulation for design at schematic level as well as at layout level is performed using ADS tool. The designed layout is fabricated, assembled and tested for desired specifications.

II. DTRM ARCHITECTURE AND REQUIREMENT SPECIFICATIONS

Most of T/R Modules employ an architecture as shown in fig1 which usually consists of Common Arm, Transmit chain, Duplexer, Receive Chain, Power Supply, Control and Timing circuits.

The Transmit chain of the T/R Module provides the required output power to the radiating element of an Antenna array and Rx chain receives a low level signal from antenna element and provides low noise amplification of the signal. A Digital Phase Shifter, Attenuator and T/R Switch together constitute the Common Arm. The Phase shifter helps steer the beam in the desired direction, while an Attenuator helps

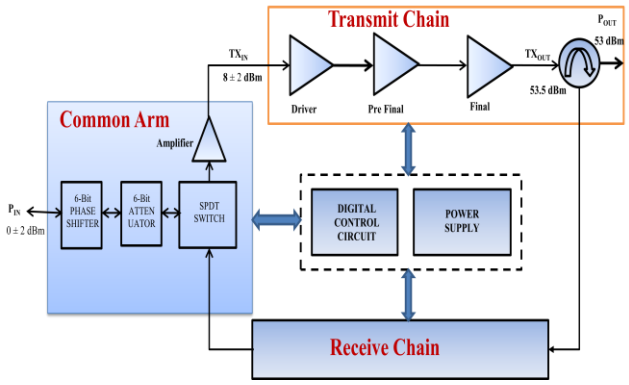

Figure 1: Single TRM Functional Block Diagram inside a DTRM.

to serve the purpose of amplitude tapering to reduce side lobe level. The T/R switch facilitates a toggle between Transmit and Receive modes. Duplexer connects to either transmit or receive while isolating the other path. There is one power conditioning card in each DTRM, which ensures availability of regulated DC voltages required by different components in the T/R Module. On the other hand, Control circuitry takes care of proper sequencing, stimulus, timing and status monitoring of power supply, temperature and forward power. Main DTRM specifications are shown in Table 1. These specifications are arrived at after Radar system analysis.

Frequency	L Band (F_0±100MHz)
Transmit I/P Power	0± 2 dBm
Transmit O/P Power	200W Peak min.
Pulse Width(Tx mode)	200 µSec at 20% duty cycle max.
Power Droop (Tx mode)	0.8 dB max.
Harmonics(Tx mode)	20 dBc min.
Receive Gain	30± 2 dB
Receive Noise Figure	3.5 dB max.
I / O Return Loss	Better than10 dB
RF Preselector Filter Rejection	Better than 30 dBc Rejection at f_0+300 MHz and f_0-300 MHz
Module Efficiency	35% min.
DC Supply	50V± 2
Dimension	230 mm× 90mm×35mm typical

Table 1:Dual Transmit Receive Module Specifications

III. TRANSMIT CHAIN DESIGN

To proceed with the Transmit (TX) chain design it is necessary to come up with and decide the number of amplifier stages to fulfill our specifications. This is accomplished by Power budgeting. This helps to zero in the number of stages and the choice of Power Amplifier devices. A good power budgeting makes sure that each stage shall provide required power to drive the succeeding stage for amplification. Besides, each Transmit chain output stages need to be in saturation (around P3dB state) so that high efficiency is maintained along with minimal effect on its Output power against variations in input drive, ambient temperature, operational frequency etc. Fig 2 shows Transmit chain Power budgeting. Power Budgeting is done at minimum input power to cater the variation at the input port. Before finalizing the devices in the chain, simulation for power budgeting, harmonics etc. are performed in keysight's ADS software.

The Transmit chain was realized as a five stage power amplifier chain in a cascade configuration viz., Predriver Stage-1, Predriver Stage-2, Driver, Pre-Final (MPA) and Power Amplifier. These devices have been finalized considering the input and output power requirements of the transmit chain. The Predriver Stage-1, Predriver Stage-2, Driver amplifiers are InGaP/GaAs Hetero junction Bipolar Transistor (HBT) based devices. Pre Driver Stages are 50 ohm matched MMICs, whereas driver has been matched to 50 ohm using Smith Chart utility available in ADS software. In order to meet the module specifications for Efficiency, Pulse width, Duty of operation as well as dimension, Gallium Nitride (GaN) based prefinal and final stages are inevitable. MPA and PA are GaN High Electron Mobility Transistors, (HEMTs) which are not pre matched MMICs, but they have got application circuitry for the required frequency band. These application circuits have been further optimized to fit into the available size of DTRM.

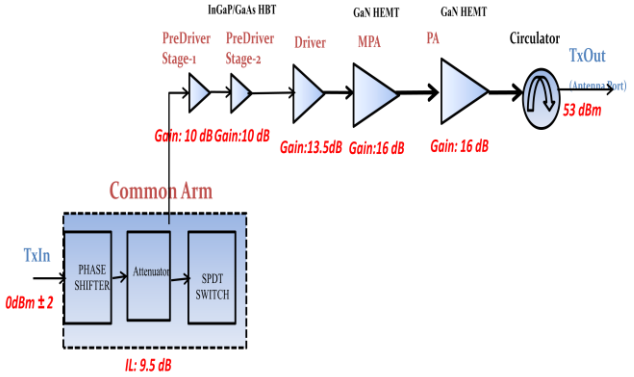

Figure 2: Transmit Chain Power Budgeting

In order to meet EMI standards at system level, Harmonic needs to be as low as possible while in transmission. These application circuits have been further optimized to fit into the available size of DTRM.

IV. RECEIVE CHAIN DESIGN

There are three most important parameters in Receiver Design: 1) Selectivity 2) Sensitivity 3) Gain

Out of these parameters, *Sensitivity* is provided by Low Noise Amplifier; *Gain* is provided by different amplification stages and Selectivity comes with Band Pass Filter. The various receive parameters like Noise Figure, Gain, Out-of-Band Rejection, Input/output Return Loss and Stability are equally important for receive chain design. Hence a tradeoff is needed to be exercised among them to optimize the design. RF front end of receivers begins with Low Noise Amplifier which has a limited dynamic Range and it generally amplifies all RF frequencies delivered to the antenna. So off-frequency signals constitute a wasteful load on the RF amplifier. The amplifier circuits also have a limit to the amount of incoming RF energy they can handle without overloading. Due to non-availability of narrowband LNA for the operating Frequency Band, preselector/ BPF needs to place before LNA. Miniaturized Micro strip Pseudo Interdigital BPF with Insertion loss less than 1 dB over the operating bandwidth with Rejection better than 30 dBc at 1.5 Bandwidth away from center frequency is designed. The response of BPF is depicted in figure3.

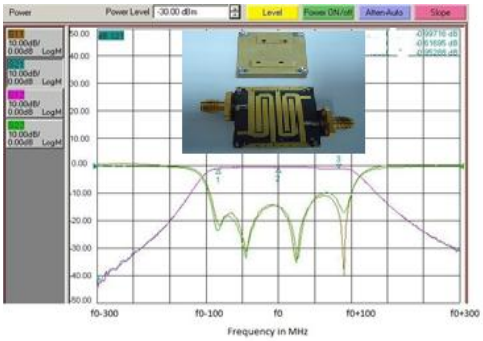

Figure 3: Measured Result of Preselection BPF

As the receiver front end (i.e. LNA) ,being an active design ,has low damage level (< 20 dBm) ,it needs to be protected against all reflections from Antenna while in

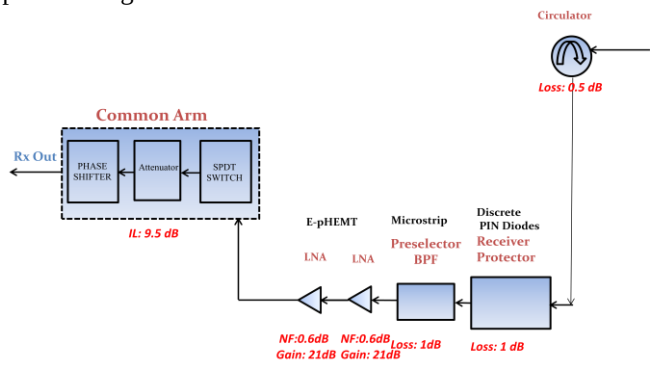

Figure 4: Receive Chain Power Budgeting

transmit mode as well as against wideband CW jammer signal when in Rx mode. In the proposed TRM design 3-stage discrete PIN diodes with shunt mounting have been implemented in switched configuration. Switched configuration is popular as very little power is dissipated by the diodes itself, thus permitting small devices to control relatively large amounts of microwave power. Reflected power is routed to the other path of switched configuration which has got high power load as well. Fig 4 shows Receive chain Power budgeting. LNA has been chosen which provides nominal Gain with minimum noise Figure along with single supply operation and high OIP3.

Complete RF receive chain is simulated in EM environment for important parameters like Gain, NF, OIP3 before realization.

V. DTRM CONTROLLER, SWITCHING CIRCUIT AND POWER CONDITIONING CIRCUIT DESIGN

Various controls and commands are needed for DTRM functionality from higher level controller as part of distributed architecture implemented in the Radar system. ACTEL FPGA based controller card has been implemented to provide the required Phase Shift for 6-Bit Digital Phase Shifter and Attenuation for 6-Bit Digital Attenuator of both channels in Transmit or Receive mode controlled by the System . It also generates various health monitoring bits like voltage, temperatures for high power dissipating devices, threshold RF level detection etc. useful for proper operation of complete system . The communication between DTRM controller and its upper level controller is carried out on Differential interface.

Same Controller PCB employs the functionality for generation of various voltages required for different devices / circuits in DTRM. Moreover, it has got protection features like over voltage, overcurrent, transient etc. At DTRM input supply connector, only one DC supply of +50V is available. With the application of a DC-DC Converter, dual outputs of +5V and -5V are available for the entire design. Separate regulators have been employed to provide the various constant voltages for digital circuit's functionality.

As Tx chain is designed with GaN based power devices, (it needs –ve voltages for Gate control as well as gate needs to be switched between pinch off potential and quiescent point) , transistor based Gate switching circuitry have been designed in order to provide fast switching as well as low power consumption. As part of power consumption reduction plan and to suppress any unwanted oscillation, LNA in receive chain and predriver stages along with Driver in transmit have been provided with their supply switching circuits.

Further, bias sequencer circuit needs to be implemented if proper operation of GaN devices has to be ensured. Power FET based circuit has been implemented to make sure Drain supply of +50V is applied to GaN power devices only after the Gate voltage availability.

VI. DTRM CONFIGURATION

Complete DTRM architecture has been divided into three boards: 1). 2-layer RF Transmit Card 2). 2-layer RF Receive Card 3). Multilayer Card. More Heat Dissipating components of DTRM have been placed in 2-layer RF Transmit Card which is closest to the cold plate. Another RF

card (Receive Card) consists of complete receive chain with common arm. Same receive card has also got pre-driver stages of transmit chain. Multilayer card is 10-layer board which includes power conditioning circuit along with FPGA control circuit.

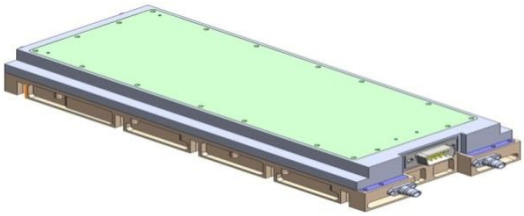

Figure 4: 3D Model of complete DTRM

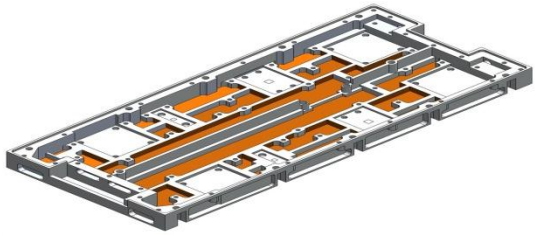

Figure 5:Top view of DTRM Transmit

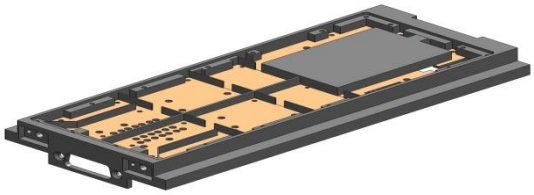

Figure 6: Top view of DTRM Receive and Common Arm

Both the RF cards are mated through BMA connectors inside DTRM. RF Transmit Card and multilayer card have been mated using D-type connector. Complete Modeling and realization of DTRM is done in-house and final 3D model shown in Figure 4, 5&6.

VII. DTRM MEASURED RESULTS

DTRM PCBs and mechanical enclosure were realized in-house as per design. Transmit Chain was evaluated at maximum duty and pulse width over the frequency band. Since there is high power attenuation at the output, it needs to be compensated in the measurement. Figure7 shows the pulse profile of transmit output at center frequency (f0). Measured transmit output power is more than 54dBm with less than 0.5 dB power droop. The oscillation from DTRM usually reflects when transmit predriver stages are blind mated to main 3-stage transmit card and gets suppressed significantly with the proper usage of absorbers.

Receive chain is characterized for important parameters like Noise Figure, Gain , return loss at Input/output and rejections at out-of-band frequencies . Figure 8 shows the final measured results for receive chain. All parameters met the specifications except Gain which needs to be

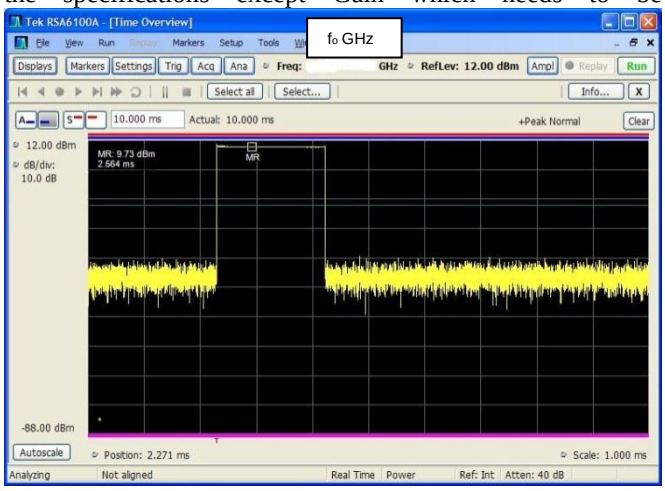

Figure 7: Measured Transmit Output Power@F0 GHz

increased by 2 dB .It can be easily done by replacing Gain stage with another device which gives 2 dB more gain.

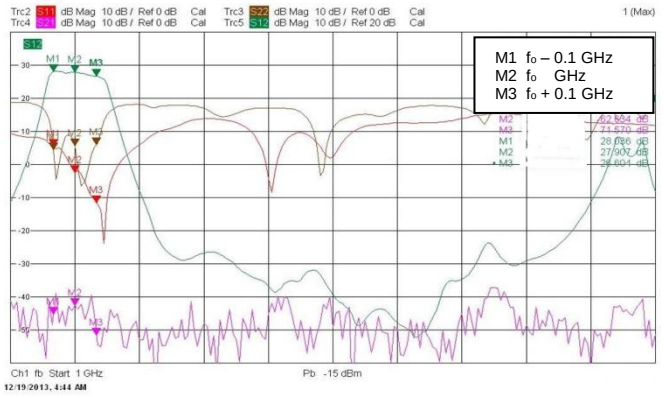

Figure 8: Measured Receive Chain S-Parameters @F0 GHz

V.CONCLUSION AND FUTURE SCOPE

Dual Transmit Receive Module with desired characteristics has been designed and developed in-house. After evaluating complete module thoroughly , it is found that major parameters like peak power output , efficiency, power droop, noise figure, return loss were achieved

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BIO DATA OF AUTHORS

Swaraj Varshney received his B.Tech. Degree in Electronics and Communication Engineering from JSS,Noida in 2008. He is working as Scientist in LRDE(DRDO), Bangalore from 2009.His present area of work are Phased Array Antenna and Transmit/ Receive Module for Active Aperture Array Radar. During T/R Module development activity, he has designed active and passive components like LNA, Switch Limiter, Filters , Coupler, various switching circuits etc. Currently, he is working in the development of solid state high power transmitters and different bands of TRMs.

Mr. Rajashekhar Chowhan P received his B.E in Electronics and Communication Engineering from Osmania University in 2006. Later he went on to receive his Masters Degree in Microelectronics from Indian Institute of Science, Bangalore. Currently,He is working as a Scientist at LRDE, Bangalore under the Ministry of Defence. His research areas include RF Microwave Circuits, Transmit Receive Modules for Phased Array Radar Systems.

Chandan Kumar received his BSc Engg. Degreein Electronics and Communication Engineering from BCE Bhagalpur in 2005. He is working as Scientist in Defence Avionics Research establishment, DARE(DRDO), Bangalore from 2007.His present area of work are design and development of RF and Microwavesubsysytems particularly Transmit/ Receive Module for Active Aperture Array Radar. During T/R Module development activity, he has designed Active andPassive components like LNA, Power Dividers, and Filters etc.

Somsing Rathod received his B.E degree in Electronics and Communication ngineering from Karnataka niversity, Dharwad in 1999 and he has completed M.Tech in Radio Frequency Design and Technology from Indian Institute Of Technology, Delhi. He is working as scientist in LRDE, Defence R&D Organization (DRDO), Bangalore since 2002. He has been working in the area of distributed beam steering controller for active phased array for airborne radar and his interest lies in design and implementation of digital systems using programmable logic devices.

Benoy Kuriakose, a research scientist,at LRDE, Bangalore, received his B.Tech. degree in Electronics and Communication engineerin from M.G. University, Kottayam, Kerala in 1994. He joined LRDE in 1999 and is working in the Air Defence Program.His intersts includes the active phased array antenna , T/R Module, Radar Exciter/ Receivers, Antenna Vehicle Controllers, Pedestal Controllers, Automated Test Equipment etc.

K Sreenivasulu received his Diploma in ECE Engineering from S V Government Polytechnic Tirupati (AP) in the year 1997. He received his B.TECH degree from Jawaharlal Nehru Technological University, Hyderabad, in the year 1995. He received his M.E degree in Microelectronics systems from IISc, Bangalore in the year 2004. He started his professional as electronics assistant in Civil Aviation Dept. where he worked from 1990 to 1995. At present, he has been working in LRDE, Bangalore as a scientist since 1996. His area of work has been in design, development of RF and microwave subsystems, digital radar systems, beam steering controller for active aperture array radar. His interest includes VLSI systems and programmable controller.