SoC FPGA based design realization of Dynamic Digital Beam Synthesizer for AESA Radars

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***Abstract*— The demand for dynamically reconfigurable digital beam synthesizer with miniaturized architecture to meet operational requirements of AESA radars has increased in the recent times. Complexity of integrating different processing elements, communication protocols and interfaces complicates the system design methodology which indeed calls for optimization of hardware and software to meet system requirements. This paper presents a customized architecture, to fit in 96 channels real time multi beam processing, high speed data communication, health monitoring, built in self test and diagnosis capabilities on a single SoC-FPGA chip with a special feature of dynamic beam weight configuration. This architecture provides enhanced functionality, adaptability and performance coupled with board space, power and system cost savings.**

***Keywords*— AESA Radar, beam forming, digital beam synthesizer, SoC FPGA, ARM processor, AXI protocol**

I. INTRODUCTION

Digital Beam Synthesizer for AESA radars requires combination of high-level computational capability of processor and stringent real-time operations of an FPGA.The proposed architecture is fusion of these two hard cores into a single embedded computing platform [1] blended with enhanced feature of Dynamic beam weight configuration for agile beam formation. The realised prototype is a single SoC FPGA [2] based card with 28nm FPGA and dual ARM Cortex-A9 MPCore Processor handling high speed data rate up to 10 Gbps. Dynamic configuration of weights and subsequent complex beam computation takes place hand in hand with processing divided partially between FPGA resources and dual core ARM Processor. Multi tasking and dynamic thread scheduling with high speed AXI Bridge between FPGA and ARM Processor makes it possible to achieve required performance [3].

II. FUNCTIONAL OVERVIEW

Real time processing of high-speed input data from active array with dynamically configurable beam coefficients is aptly distributed between high-end FPGA and ARM processor of the SoC device[4]. Dedicated multi-threaded software application is responsible for beam weight calculation and configuration based on command received from radar controller. An interrupt service routine implemented in kernel space gets activated on reception of command and instructs processor for calculating weights on high priority. Ping pong buffers [5] have been used to implement simultaneous weight configuration for next burst during real time data processing of current burst. Dedicated high speed data link between FPGA and ARM makes it possible to achieve required operational performance. The functional block diagram representing the fused architecture for dynamic digital synthesizer is depicted in *Figure 1.1*.

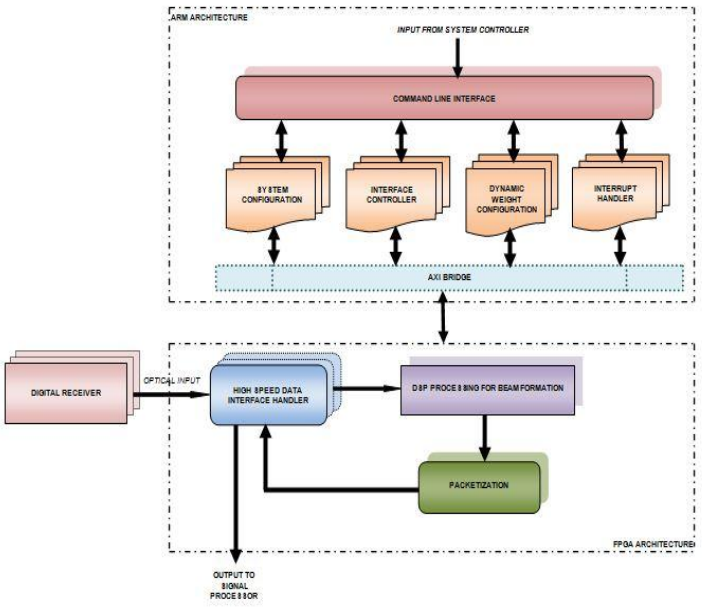

Figure 1.1: Block Diagram of SoC based Digital Beam Synthesizer

III. DYNAMIC BEAM WEIGHT CONFIGURATION

Processor based calculation of weight coefficients is implemented in the proposed architecture as explained above. Reconfigurations of weights results in dynamic updation of receive beam pattern formation, thereby introducing beam agility from burst to burst.

The weight coefficient for nth sample of beam steered to angle Ø is given as [6]:

$$w_n = e^{j2\pi\frac{d}{\lambda}(n-1)sin\,\phi}$$

On reception of waveform parameters like transmission frequency, beam type & array parameters pertaining to next burst, beam weights are re-calculated at software level & new coefficients are loaded onto memory blocks accessible by FPGA. The beam corresponding to IQ data of next burst is hence dynamically formed.

The benchmarking of time consumed for computing beam coefficients on the fly with this fused architecture is given in *Table 1*. The simulations and observations have been carried out in Matlab© and ARM DS-5 IDE.

TABLE I
DYNAMIC BEAM WEIGHT COMPUTATION PERFORMANCE

Updation Time of Beam Coefficients (ms)				
Trial#1	**Trial#7**	**Trial#13**	**Trial#19**	**Trial#25**
0.168	0.167	0.168	0.167	0.167
0.168	0.167	0.169	0.166	0.167
0.168	0.167	0.167	0.166	0.164
0.172	0.168	0.166	0.168	0.167
0.189	0.166	0.168	0.171	0.171
0.166	0.171	0.17	0.168	
Average Time (ms)				**0.168**

The average time taken for computation & loading of beam weights for 8x12 array architecture is about 168us as shown in *Figure 1.2* which is sufficiently well before the start of next burst scheduled in most of the Radar systems[7].

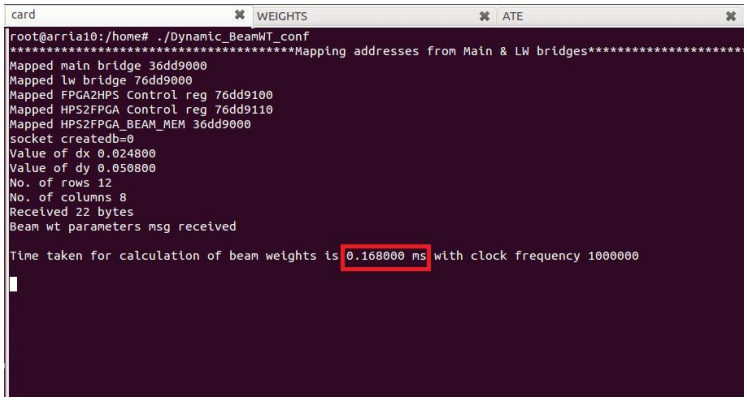

Figure 1.2: Dynamic Beam weight computation performance

The MATLAB simulated beam generated for 8x12 array with transmission frequency of 3.1GHz & steering angle 0º in azimuth is shown in *Figure 1.3*.

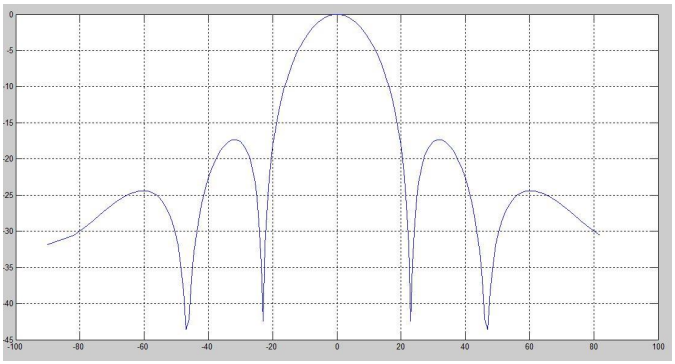

Figure 1.3: Simulated Beam for 8x12 array with centre on boresight

The beam synthesized by dynamic digital beam former with same transmission frequency and antenna array configuration but steering angle set to 5º is shown in *Figure 1.4.*

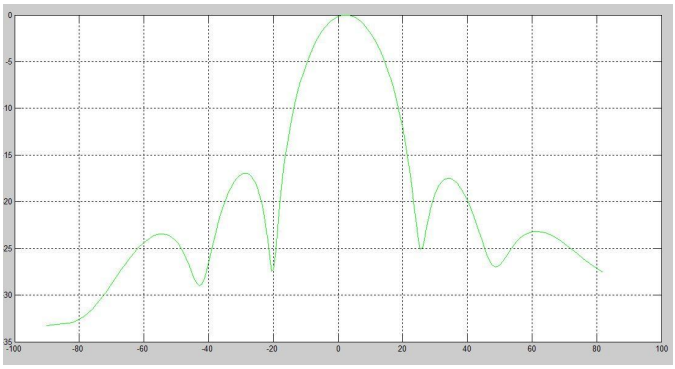

Figure 1.4: Digital Beam Synthesizer for 8x12 array steered at 5º in azimuth

IV. HARDWARE IMPLEMENTATION

Beam synthesizer card is realised on 3U PCB and comprises of following components

- Single SoC FPGA
- Optical Transceivers
- DDR3 RAM
- 10G Ethernet
- Backplane connector
- Other debug peripherals

The individual module and the whole set-up housed inside a chassis for 96-channel array configuration is shown in *Figure 1.5.*

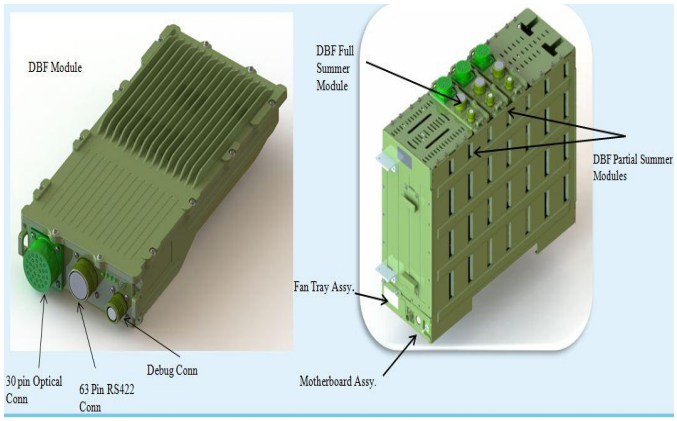

Figure 1.5: Hardware Model of Digital Beam Synthesizer

V. SOFTWARE IMPLEMENTATION

- Embedded Linux[8] kernel 3.10.31-ltsi installed with FPGA drivers for resource sharing between the FPGA and ARM Cortex-A9 processor AXI bus protocol [9] .
- Slow peripherals such as registers for control and status of the beam formation are connected via AXI lightweight bridge
- Memory blocks for dynamic configuration of beam coefficients and storing complex beam output are interfaced through high speed AXI master bridge.

The software architecture is depicted in *Figure 1.6.*

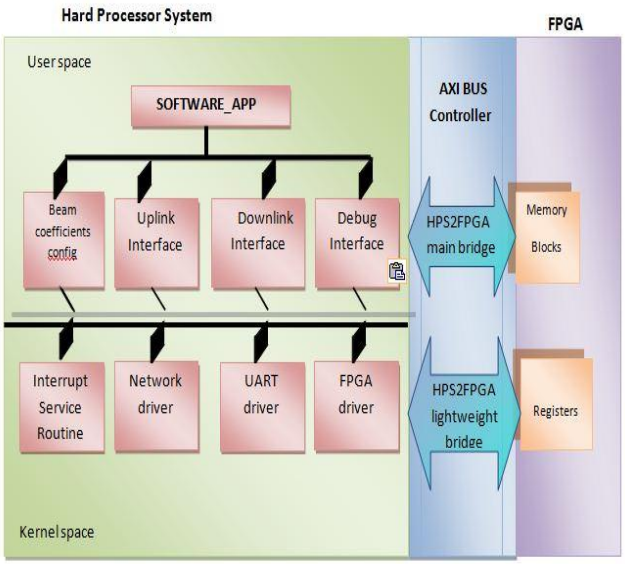

Figure 1.6: Software Architecture of Digital Beam Synthesizer

VI. SALIENT FEATURES

- Dynamic Weight configuration for beam formation.
- Modular and scalable architecture to cater generic solution for various configurations of Phase Array Radars
- High speed data handling capacity up to 10Gbps per link.
- Power efficient solution with 20 W power per card.
- Compact mechanical design.
- Cost effective solution

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VII. CONCLUSION

This architecture provides increased adaptability due to agility incorporated at beam data calculation and configuration, power and cost reduction as well as future proofing the design unlike conventional architectures with fixed beam coefficients. The same design approach can be adopted for other logic intensive systems of AESA Radars like adaptive beam formers, Signal Processors and Radar Controllers etc

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