Development of Indigenous On Board Controller (OBC) ASIC for Space-borne Synthetic Aperture Radar (SAR)

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Abstract:

This paper describes* design and development of *Indigenous On Board Controller (OBC-2.2) Application Specific Integrated Circuit (ASIC), which has been developed for ISRO's various Space-borne Synthetic Aperture Radar (SAR) missions. OBC ASIC is used in T/R controllers(TRC) to control T/R Modules (TRM) for electronic beam steering. The OBC ASIC is based on 8 bit micro-controller soft IP core with a 32 bit IEEE 754 complaint Floating Point Co-processor (FPC). The FPC is used for real-time computation of digital phase/attenuation values for TRM from required elevation and azimuth angles. Event Programmable Serial/Parallel Interface (EPSPI) module is used for Event driven beam configuration data loading to TRMs, up to 8 TRMs can be simultaneously controlled by a single OBC ASIC. Timing Signal Re-generator (TSRG) module contains array of programmable pulse generators. There are total 6 asynchronous transmitter/receiver (UART) modules for serial communication. This mixed signal ASIC contains RS-422/485 transceiver, ADC, clock oscillator and Linear Voltage Regulator (LVR). The OBC-2.2 ASIC has been realized on 180nm CMOS process of Semi-Conductor Laboratory (SCL), India with 256 pin CQFP package. It operates at 24 MHz and dissipates less than 1 Watt. T/R Controller (TRC) sub-system based on this indigenous OBC-2.2 ASIC has been realized for ISRO's Radar Imaging Satellite (RISAT-1A).

Key Words: Synthetic Aperture Radar (SAR), Electronics Beam Steering, Distributed Controllers, Micro-controller, Floating Point Coprocessor, ASIC, T/R controllers(TRC)

I INTRODUCTION:

Space-borne Synthetic Aperture Radar like RISAT-1A (Radar Imaging Satellite) are based on active phased array radar because of it's capability of electronics beam steering, multi-beam operations, large bandwidth and high efficiency. Electronic beam steering requires real time loading of digital amplitude and phase values to the array of Transmit/Receive Modules (TRMs). For large elements array, distributed T/R Controllers (TRC) are used to load these beam characterization data, timing control and serial communication.

This paper describes design & development of indigenous On-Board Controller (OBC-2.2) ASIC to meet the requirements of the control sub-systems of SAR. The first version of On Board Controller (OBC-1) digital ASIC, flown on ISRO's RISAT-1 mission was fabricated at foreign foundry. OBC-2.2 mixed signal ASIC has been indigenously designed by team from Space Applications Centre (SAC) and Semi-Conductor Laboratory (SCL). It has been fabricated at SCL's 180nm CMOS process. OBC-2.2 ASIC is system on Chip (SoC) implementation optimized for T/R Control (TRC) application.

Section-II of this paper describes distributed controller hierarchy of SAR payload. Section-III describes T/R Controller, section-IV describes OBC-2.2 ASIC and section V describes implementation results.

II. Distributed Controller Hierarchy

The three level hierarchy of distributed controllers for RISAT-1A is as shown in figure-1. Payload Controller (PLC) is the central beam controller. PLC controls 12 Tile Control Units (TCU) which is at 2nd level. Each TCU further controls 24 Transmit/Receive Controller (TRC) which is at 3rd level. Thus, the phased array active antenna has total 288 (12x24) TRCs. Communication among distributed controllers is done through RS-422/485 serial link. PLC sends beam selection data to TCU, which further transmits beam characterization data to TRC through serial commands. TRC does temperature correction on characterization data.

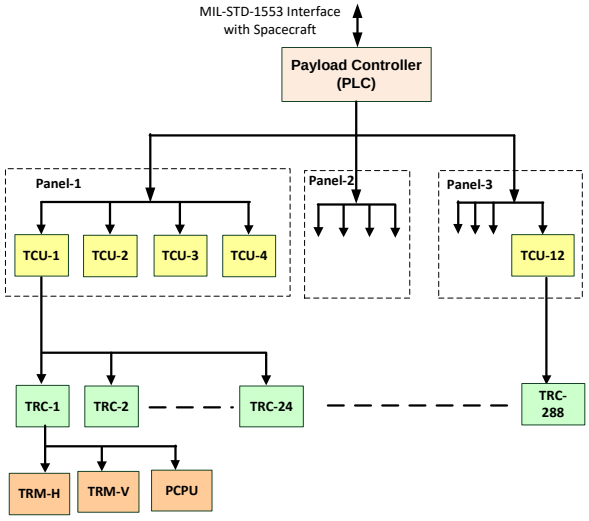

Figure-1: Distributed controllers Hierarchy of RISAT-1A

III. T/R Controller (TRC)

The functional block diagram of T/R Controller is shown in figure-2. The main functionality of TRC is to control, coordination and status monitoring of TRiM (T/R integrated Module) and associated PCPU (Power Conditioning & Processing Unit). TRC has RS-422/RS485 serial interface with TCU for command, data and telemetry. TRC also receives timing signal reference from TCU over RS-422 interface. TRC gets analog signal from thermistor of TRiM for temperature compensation. During SAR mode configuration, each TRC receives the beam-forming information (azimuth and elevation angles) from TCU. TRC loads temperature compensated attenuation and phase values to the TRiM-RF during transmit and receive cycles for all the modes of SAR operation. TRC also generates switch control signals for TRiM-RF and PCPU.

Real time Phase Computation

6 bit digital phase control for TRM is computed as per equation-1.

$$\Psi = (2\pi/\lambda)*\{d_{az}*Cos(\theta)*Sin(\phi) + d_{el}*Sin(\theta)\}$$

…Equation- 1

Where,

d_{az} = Azimuth Position of TRiM
d_{el} = Elevation Position of TRiM
θ = Elevation Pointing Angle
φ = Azimuth Pointing Angle

d_{az} and d_{el} are constant for a TRiM, based on its location of mounting on phased array antenna. It will be stored in PLC as a LUT and it will be transmitted by PLC to each TRiM separately according to TRiM ID number before start of imaging. Phase values for each TRiM is computed by Floating Point Co-processor(FPC) of OBC-2.2 ASIC to steer beam in real time.

Sine/Cosine LUT Implementation:

Equation-1 requires computation of two sine values and one cosine value. Sine/cosine values will be generated from Look Up Table. The look up table size is optimized (reduced) based on following considerations:

- Maximum Input angle (Elevation/Azimuth) range is -30° to +30°, so no need to store values for complete -180° to + 180°.
- $Sin(-\theta) = - Sin(\theta)$, $Cos(-\theta) = Cos(\theta)$, so values for only positive angles should be stored

LUT size will be 600 Words (30°/0.05°), for 32 bit floating point data type for sine value, the total LUT size will be 2400 Bytes.

OBC2.2 ASIC utilize EPSPI module, ADC module and FPC module for event based loading of temperature compensated phase values computed through equation-1 for Transmit and Receive events in each PRF. It controls events of Transmit and Receive for given mode of operation through TRMSW (T/R Module Switch control) module, by configuring the switches of TRiM and through generation of the PCPU control pulse. Linear Voltage Regulator is used for powering the core of OBC2.2 ASIC

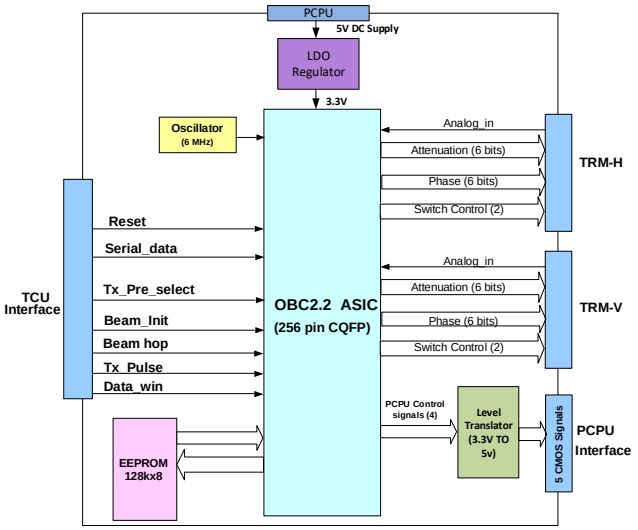

Figure-2: Block diagram of TRC

IV OBC-2.2 ASIC

Architecture of OBC-2.2 ASIC is shown in figure-3. OBC-2.2 ASIC is based on 8 bit DW8051 micro-controller soft core along with 32 bit IEEE Std. 754 complaint Floating Point Coprocessor (FPC). DW8051 is interfaced with various peripheral modules through SFR (Special Function Register) and memory bus. Specifications of OBC-2.2 ASIC is shown in table-1.

Table-1: Specifications of OBC-2.2 ASIC

Parameter	Specifications
ASIC Type	Mixed Signal
Process	0.18u CMOS
Foundry	Semi-Conductor Laboratory (SCL), India
Clock frequency	24 MHz
Supply Voltages	3.3V (1.8V for core is generated by on chip LVR)
Micro-processor	DW8051
Co-processor	32 bit Floating Point Co-processor as per IEEE 754
No of TRM ports	Up to 8 TRM ports (configurable parallel/serial)
UARTs	Total 6 UARTs (1-RS422, 3-CMOS, 2-RS485)
I/Os	179 functional I/Os, total 256 pins
Radiation Hardness	Rad Hard by Design
Package	CQFP-256
Power Dissipation	500 mW @ 24 MHz

Digital Modules:

The RTL design of OBC-2.2 ASIC has been carried out in VHDL. Each modules have been verified at module level and then integrated at top level. Following is the list of various digital modules:

1) DW8051 Microcontroller:

DW8051 is 8 bit micro-controller core is complaint to intel MCS-51 instruction set with 4 clocks instruction cycle.

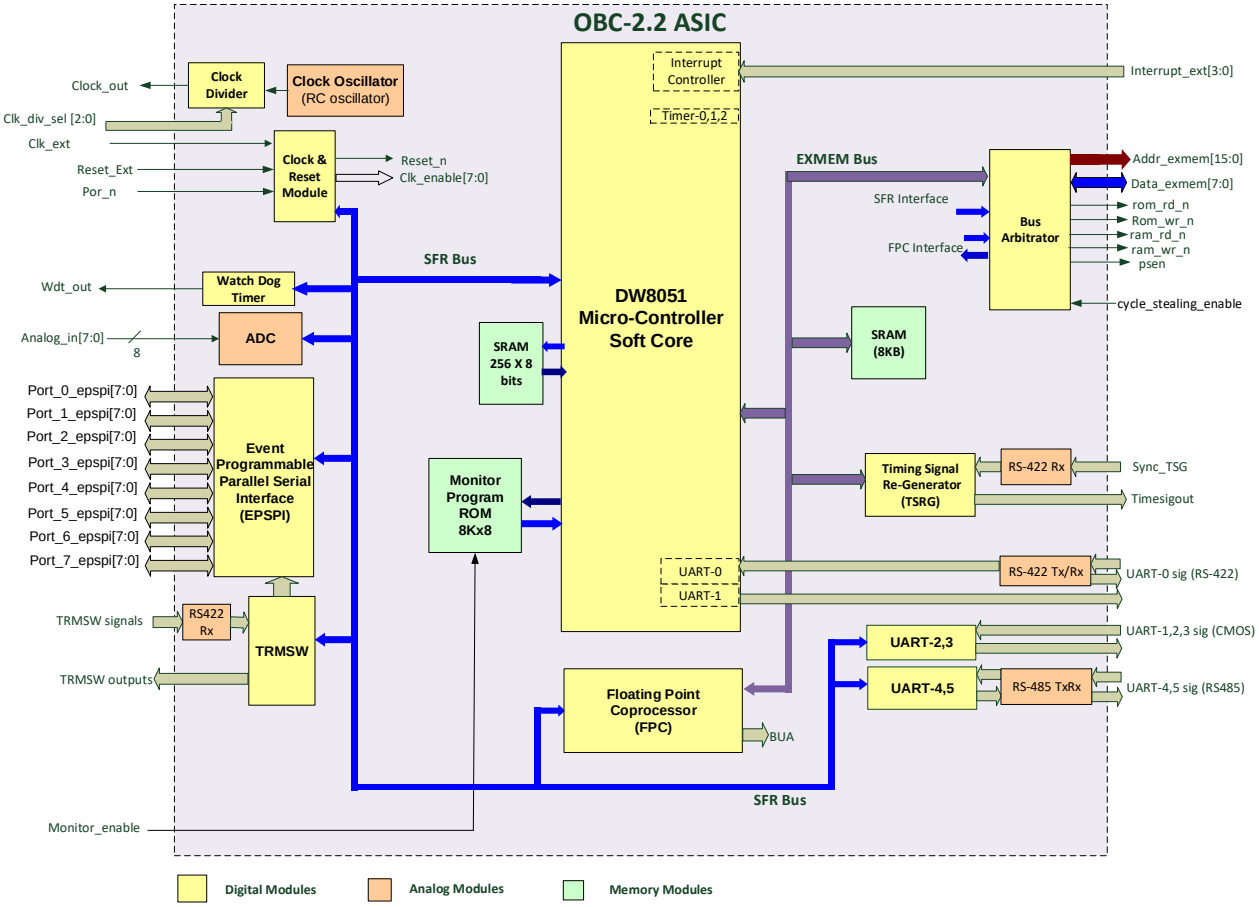

Figure-3: OBC-2.2 ASIC Block diagram

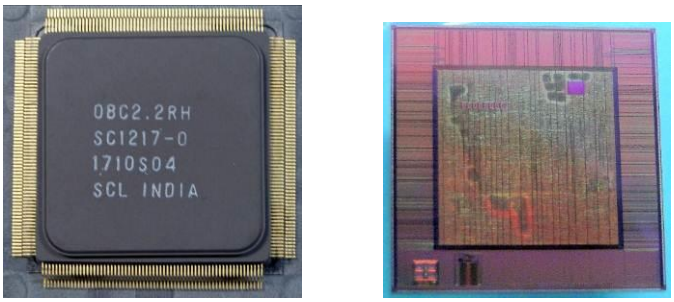

Figure-4: OBC-2.2 ASIC (CQFP-256 package & die)

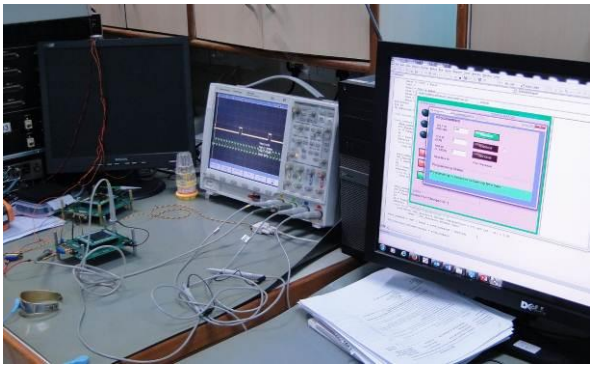

Figure-5: OBC-2.2 ASIC test setup

Figure-6: RISAT-1A TRC DVM Photograph

2)Clock & Reset Module:

It generates internal reset which is asserted asynchronously and de-asserted synchronously. It also generates clock enable signal for peripheral modules so that inactive modules can be disabled for power saving.

3)Clock divider:

This module divides on chip oscillator clock as per external pin selection.

4) Watch Dog Timer:

Watch Dog Timer generates reset/NMI (Non Makeable Interrupt) whenever the software fails to access it within specific time interval.

5) Event Programmable Serial/Parallel Interface (EPSPI):

Event Programmable Serial Parallel Interface (EPSPI) module implements parallel/serial I/O triggered by event on external timing control signals. There are total 8 ports in EPSPI, in parallel mode each port works as 8 bit parallel input/output port, in serial mode each port implements 3 wire (clock, strobe, data) SPI interface. The micro-controller writes data in the register banks, data is transferred from register banks to ports depending on Event-Action Look Up Table.

6) TRM Switch Control Module (TRMSW):

This module generates switch and pulse control signals for TRM (T/R Module) & Power supply sub-systems.

7) Floating Point Coprocessor (FPC):

This module will implement 32 bit floating point (IEEE 754 standard) arithmetic functions like addition, subtraction, multiplication, division.

8)Timing Signal Re-Generator (TSRG):

This is generic timing signal generator, which can generate up to 8 programmable pulses with ON and OFF programmable duration. Each signal can be generated with sync or as free running or in toggle mode.

9)UART:

There will be total 6 UARTs in OBC-2.2 ASIC, out of which 2 will be DW8051 internal UARTs and 4 UARTs will be implemented external to DW8051 with SFR interface.

10)Bus Arbitrator

This module implements bus-arbitration logic to access external program & data memory.

11)Monitor ROM:

The ASIC operates in monitor mode, when monitor_enable pin is set to high at reset. This mode is used for debug and "in-circuit programming" of EEPROM through UART serial interface.

Analog Modules:

1) RS422 Differential Receiver/ Transmitter

RS-422 Receiver/Transmitter convert differential signals to single ended as per RS422 standard.

2) RS485 Transceiver

RS-485 half duplex transceiver for conversion of differential signals to single ended as per RS485 standard.

3) Power on Reset Generator

This module will generate low level pulse of 40 us at power on to bring the digital module to a known state.

4) Clock Generator

This is a ring type clock oscillator to generates clock of frequency 24 MHz.

5) Analog to Digital Converter (ADC)

This is a sigma delta type 24 bit ADC with sampling rate of 160 KHz with 8 channel analog mux.

6) 3.3V to 1.8V Linear Voltage Regulator

It is a hard IP, which is used to generate 1.8V from 3.3V supply, which is required for digital core and IOs. It can supply up to 150 mA current.

V. Results

Functional Verification

Functional Verification of OBC-2.2 design has been carried out with DW8051 as a central processor. Individual test benches are developed for all the modules of OBC ASIC. Figure-7 shows the Block diagram of Functional verification environment of OBC ASIC.

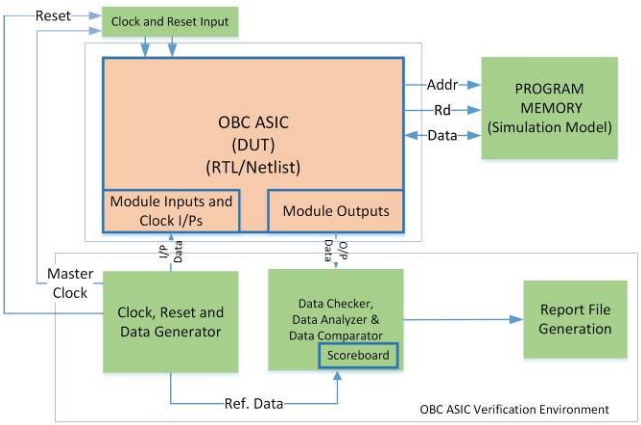

Figure-7: Top level verification environment

OBC ASIC digital core is verified by an automated testbench. The test strategy covers verification of each SFR or Memory Mapped modules of OBC ASIC for all the modes of operation independently. A separate Data checker unit developed which accept the input from DUT as well as test benches. Data checker unit compares the both the inputs and generate the report file to indicate the pass/fail of test case. The test cases at the top-level consist of assembly/C code as well as the VHDL test procedures. Assembly/C code is required for 8051-core programming and VHDL test procedures are required to generate test-vectors for the modular interfaces as well as data checker. Program memory is initialized with a test case program. Once reset is removed from OBC ASIC, it fetches the instruction from a Program Memory.

Functional verification has been carried out at different design stages; RTL Level, Synthesized Netlist Level, Pre Layout Netlist and Post Layout Netlist Level. Timing Simulation has also been carried out on Post Layout Netlist.

Total no of module level test cases	950
Total no of top level test cases	300
Code coverage	>97%
Total simulation run time	7-8 seconds

ASIC implementation results:

OBC-2.2 ASIC digital core has been synthesized using SCL developed logic library. Digital design contains

internal scan chain for manufacturing test after wafer fabrication. Following table shows major implementation results.

Gate Count	132K (nand2 equivalent)
Max clock frequency	24 MHz
Scan Chain length	Chain-1 : 8366, Chain-2:718
ATPG test coverage	99.55%
Die Size	14.472 mm x 14.472 mm

The OBC-2.2 die has been packaged in standard CQFP 256 pin package. OBC-2.2 ASIC has been functionally tested on a customized test board, figure-5 shows test setup. OBC-2.2 ASIC has been mounted on RISAT-1A TRC DVM board as shown in figure-6, it has been successfully tested for TRC functionality.

CONCLUSION

Indigenous On Board Controller (OBC-2.2) ASIC has been described in this paper. OBC-2.2 ASIC is developed for use in T/R controller (TRC) of Synthetic Aperture Radar (SAR) payload of RISAT-1A satellite. The OBC-2.2 is mixed signal ASIC with digital modules like micro-controller core, floating point coprocessor along with various peripheral modules and analog modules. The OBC-2.2 ASIC has been realized on 180nm CMOS process of Semi-Conductor Laboratory (SCL), India with 256 pin CQFP package. T/R Controller (TRC) sub-system based on this indigenous OBC-2.2 ASIC has been realized and successfully tested. Indigenous design & fabrication of such critical component makes ISRO self-reliant in realization of various space missions.

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