Design & Development of Hardware and Software for waveform and trigger generation for Receiver of RAWL 02 MK IIA Radar

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Abstract:

The Waveform & Trigger Generation Unit is designed and developed for generation of programmable IF 30 MHz expanded pulse, various waveforms required for Radar operation and synchronization triggers for Receiver, Signal processor and Transmitter of RAWL 02 MK II A radar. RAWL 02 MK II A is state of the art Solid-state coherent 2D air surveillance Radar for L Band application. Radar is operational in Myanmar.

Key Words: Pulse compression, IF 30 MHz expanded pulse, LFM, co-efficient, RHEL platform, firmware, Triggers, Radar Controller, PRF

I INTRODUCTION

The Radar RAWL-02 MK-II A is a Coherent Radar which provides a detection volume space up to 160 Kms in range, elevation coverage of 40° and 360° in bearing and provides video signals for display purposes and as well as tracks for target track generation. The design is aimed at providing a high performance, technologically superior long range L Band air surveillance, Coherent Radar RAWL-02 MK-II A, which is suitable for installation onboard large and medium size Naval Ships and onshore establishments.

RAWL-02 MK-II A Receiver is a state-of the art system which is based on the latest technology available. Waveform & Trig Gen Unit (WTG) is heart of the radar system with latest technology modules used.

Waveform & Trig Gen Unit (WTG) is FPGA based hardware DAC which generate 30 MHz chirp pulse for transmission with 5MHz bandwidth, LED pcb for indications of the supply, clock and triggers and a mother board for reducing the complexity of the wiring and interface to the connectors housed in a housing.

Hardware has ethernet interface via which online controls of pulse profiles are received based on modes of radar and hardware generates the triggers and chirp waveform real time synchronized with system clock. LFM signal leads to advantage of low transmitter power, better range resolution, higher bandwidth and better interference rejection.

II FUNCTIONAL DESCRIPTION

WTG is state of the art design and is multifunctional module which has various functionalities as listed below:

- The Module generates IF chirp expanded pulse signal with LFM of 5 MHz bandwidth for 4us, 75us and 150us.
- Generates real time Triggers required for Radar operation for synchronization of transmitter, receiver and signal processor modules.
- Generates Gate pulse for switching ON SSPA Transmitter.
- Accepts control and command in real time from Radar Controller for generation of Chirp waveform and system triggers.
- Generates triggers required by Radar monitor for forward and reflected power measurement.
- Generates triggers required by signal generator for performing calibration checks using signal generator.
- Monitors Antenna Heading line and Bearing pulses which is used as trigger to generate pulses.
- Simulated targets can be generated having the same profile as LFM useful for fine tuning of radar.
- Command controlled sector transmission feature.

III HARDWARE DESCRIPTION

Hardware is a compact box realization. Box (figure 1) houses FPGA Board, mother board with blind mating connectors, LED board with LED indicators and signal monitoring points. FPGA Board is indigenously developed 12 layer PCB consisting of Xilinx Virtex 5 FX series (XC5VFX70T-1FFG1136I) FPGA which includes the Power PC hardcore IP and board consists of various hardware interfaces like UART interfaces (Four channel RS232 and RS422), Two Gigabit Ethernet interface, Differential I/O for generating Triggers, TTL signal interface, 32 MB NOR flash and 128 MB DDR2 SDRAM.

Figure 1 WTG Hardware

The hardware also consists of 16 bit ADC with Eight channel multiplexer for monitoring analog signals, Four channel 14 bit DAC with 40 Msps DAC for generation of arbitrary analog waveform over SMA, Two channel 14 bit DAC with 160 Msps speed is available for generating IF of 30 MHz expanded chirp waveform using 400 MHz external sampling clock on SMA. Hardware also has on board 100 MHz oscillator and Eight channel 16-bit ADC with sampling rate of 1 MSPS.

The board is powered from single 5V power input from backplane connector via motherboard. Board is designed to fix in a specialized designed mother board chassis's. The board is standard double euro size with a front fascia and two mating connectors at the rear. Mother board translates VME connections to blind mating D-type connections. LED board brings out various signals indications and also few test points from main board. Compact box is rugged with EMI/EMC protected and is in standard form factor.

IV SOFTWARE DESCRIPTION

Software is developed in VHDL and embedded C. XILINX ISE is used for VHDL logic development. VHDL logic includes real time generation of Triggers with parameters adapted based on various radar operating modes.

RHEL platform is used for embedded C firmware development which runs on power pc. uLinux is chosen for porting on power pc. The uLinux has driver files for various external hardware interfaces. The binary files like uRamdisk, uBoot, Device binary tree and uImage are generated and flashed for interfacing firmware with VHDL logic along with all external interfaces.

VHDL RTL logic generates all system triggers and chirp waveform with respect to 400 MHz clock and antenna heading line. RTL logic receives HL and Bearing signals from antenna and computes the instantaneous angle. RTL logic also takes care of changing pulse chirp based on pulse width and PRT details got by firmware.

Firmware has UDP portion for communication with Radar controller. Firmware receives the commands real time from Radar controller and sends to RTL logic for waveform and trigger generation online.

Firmware sends angle information to RC via LAN. Firmware acts on control packet received from RC and responds with acknowledgment. Firmware sends status packet consisting of chirp signal status, PRT and Pulse width characteristics, HL and Bearing status on request to status request packet received from RC.

V IMPLEMENTATION

RTL logic is synchronized with Antenna signal and 400 MHz clock is used as reference for generation of all system triggers and pulses required by transmitter, receiver and signal processor. 140 Msps DAC is used to generate LFM chirp signal.

Pulse expanded chirp signal of 4us, 75us and 150us is generated with LFM at 5 MHz bandwidth. up chirp from 27.5 MHz to 32.5 MHz is been generated. Chirp signals are generated in real time, based on commands received from Radar Controller. For generating chirp, external 400 MHz clock is interfaced with FPGA. FPGA generates control signals and 14 data bits required for 160 Msps DAC. Two such DACs are interfaced for actual chirp generation and for simulated target signal generation.

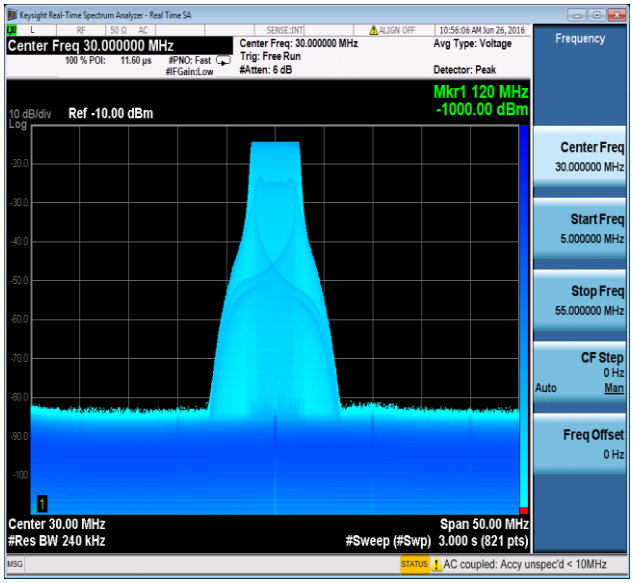

Figure 2 Frequency spectrum domain

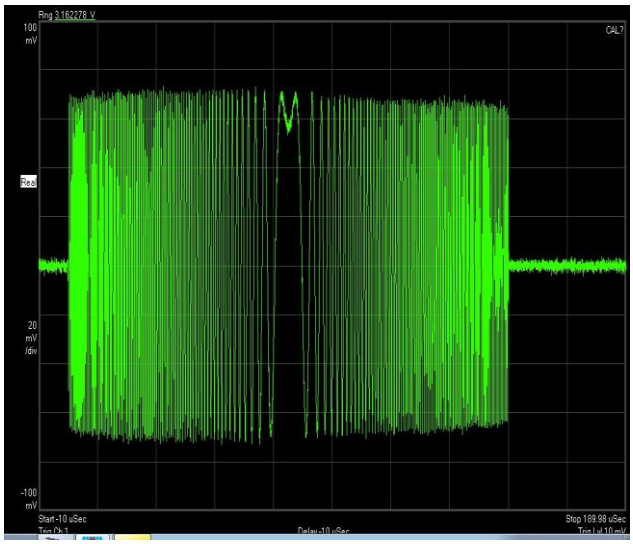

Figure 3 Chirp signal-time domain

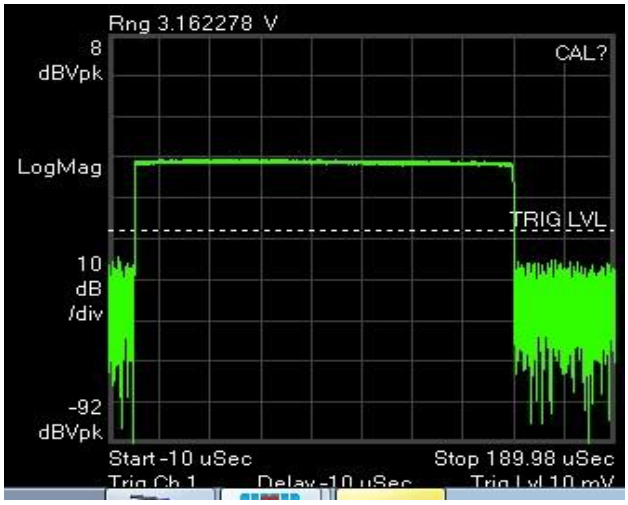

Figure 4 Frequency v/s Time

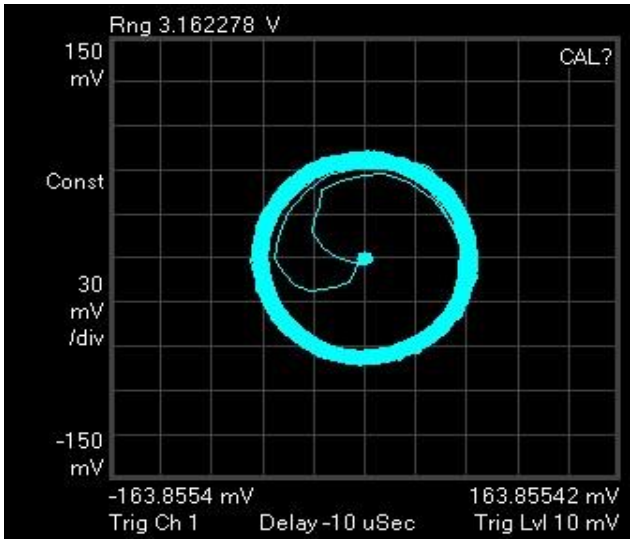

Figure 5 Chirp signal – 1 and Q plot

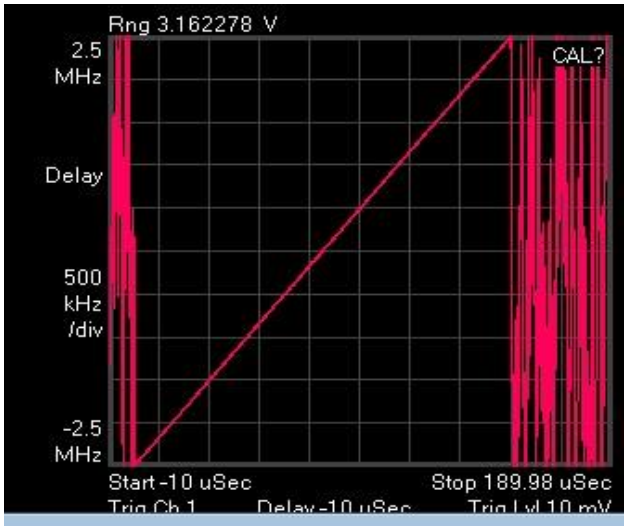

Figure 6 Chirp signal frequency

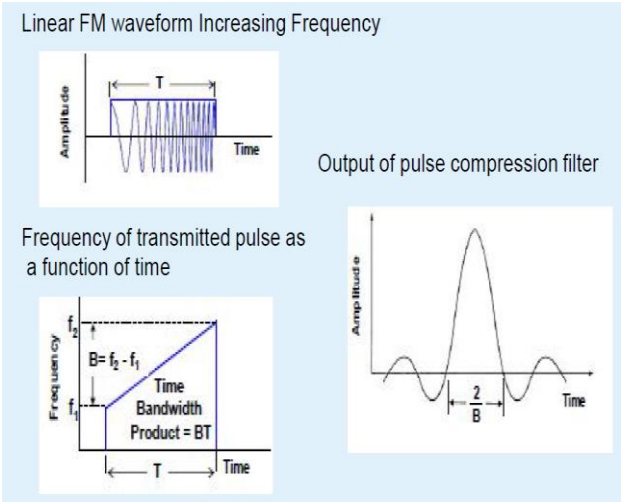

Figure 7 LFM expansion and compression

Mathematical algorithm is used to find the co-efficient of expanded chirp pulse and those values are stored in ROM blocks and Soft filter is used for removal of harmonics. The functional blocks required for chirp generation are designed using MATLAB Simulink tool. The functional blocks are DDS core, ROM, Band pass Filter and scalar modules. The designed logics in MATLAB are ported to FPGA. The interface logic, AND computation logic for generating co-efficient for DAC is handled by firmware.

LFM expanded pulse is generated by VHDL logic generates LFM of short pulse 4 us followed by long pulse 150us during antenna rotation of 5RPM. It also generates LFM of short pulse 4 us followed by long pulse 75us during antenna rotation of 10RPM. The PRT for both rpm varies based on staggered and non-staggered prf combinations, which is again generated real time as and when command received from Radar Controller. The waveforms generated are all programmable via command initiated from RC.

Chirp signal generated from WTG is captured and analyzed by Real time spectrum analyzer, screen shot is as shown in figure 2 - spectrum of chirp signal, figure 3 - Time domain of chirp signal, figure 4 - frequency domain of chirp signal, figure 5 - I and Q plot of chirp signal, figure 6 - LFM frequency slope of chirp signal. Expanded LFM pulse on reception is pulse compressed to achieve the advantage of more bandwidth and better target resolution as shown in figure 7.

Apart from system triggers and LFM pulse WGM has various other functions:

WGM generates simulated Targets for verification and testing of entire radar sub-system. Targets which are stationary, moving up to 3 mach speed can be generated with option of Doppler variation. All the parameters which are received from RC is as show on a GUI figure 8. Parameters like pulse width, PRT, PRF, Radar modes, RF on/off, TX on/off and sector transmission on/off is settable from RC.

WGM also has feature of sector transmission in which triggers are withdrawn during sector blanking. WGM also generates Noise trigger required by Radar monitor to measure forward and reflected power. WGM generates signal generator trigger required to interface signal generator during calibration.

Figure 8 WGM parameters controlled by GUI

CONCLUSION

This paper explains about indigenous design and development of waveform and trigger generation module. The Functionalities, Hardware details, Software details, Implementation methodology and Test results of WGM module. WGM is operational in the Radar RAWL-02 MK-II A deployed in Myanmar onboard ships F-14 and 773 for Royal Myanmar Navy and deployed at INS Dronacharya for Indian Navy. The WGM can be adopted for similar Radars because of online and real time controllability.

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