2 kW Tuned RF Solid State Power Amplifier at 18.1 MHz in Pulsed Mode Using Single LDMOS Transistor

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Abstract:

This paper discusses and describes the design, development and test results of a 2 kW Peak Power Solid State Power Amplifier (SSPA) in pulsed mode at 18.1MHz from an input of 10 W. In this design, we used a BLF188XR Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor. This is a High Power Extra Rugged HF/VHF (2 – 600 MHz) transistor in SOT539A package. This paper also contains the theoretical calculations, physical construction and test methodology of the aforesaid SSPA. This transmitting system is aimed to be used for the existing HF Radar System of the Space Physics Laboratory (SPL), Vikram Sarabhai Space Centre, Trivandrum. This HF Radar System is a phase coherent, pulsed, monostatic and moderately high power Doppler Radar System operating at 18.1MHz over the magnetic equatorial station, Thumba (8.5^0N, 77^0E). At present, the HF Radar uses the old vacuum tubes (EIMAC 8960 Power Tetrode Valve) based transmitter, which had become obsolete now. In this context, the use of new SSPA will not only enhance the capability of this radar, but also enable the system to be augmented using new and contemporary technology.

Key Words: Solid State Power Amplifier, HF Radar System, LDMOS

I INTRODUCTION

Conventionally, High Power Radar Systems use vacuum tube based transmitters with multiple high voltage power supplies. The disadvantages of these systems are; they are bulky, consume high power, low efficiency and the required vacuum tubes are now obsolete. In order to overcome these drawbacks, we present a spot frequency tuned Solid State Power Amplifier (SSPA) with a single LDMOS transistor. Lumped element based impedance matching and Wilkinson type power divider/combiner have been implemented at input and output stages of this SSPA. This approach generates pulsed RF output of ~2 kW peak power *(~900 V_{pp})* from a 10 W RF_{in} at *50 V* DC source.

Most of the Solid State Power Amplifiers are configured in class AB mode, but here this SSPA is configured as class-C mode. The main advantage of this configuration is that there is no need of regulated precision $V_{GS,}$ therefore, the heat generated in the SSPA is low and has low current consumption. For gate biasing a self-biasing circuit using a *VK200 RFC* is employed. Most of the Radars are working in pulsed mode, so this amplifier is suitable for pulsed Radar Systems. Here, we use tuned tank circuits for a spot frequency using variable inductor in parallel with a capacitor.

HF Radar is used for ionospheric studies and is a powerful tool to investigate the plasma instability processes prevailing in the Equatorial Ionosphere due to the phenomena, Equatorial Electrojet (EEJ, 80 to 110 km altitude) and Equatorial Spread-F (ESF, 200 – 1000 km altitude). The radar employs Doppler Beam Swinging Technique, which provides both zonal and vertical drifts of the ionospheric irregularities. The HF Radar System provides the information about the random and collective

movement of plasma bubbles in the equatorial ionosphere. It also gives the vertical movement of F1 and F2 layers of the equatorial ionosphere. For this purpose, the carrier frequency of *18.1 MHz* with a pulse width of 20 – 100 µS and pulse repetition frequency of *100 to 250 Hz* is employed. The transmitted pulse gives echoes from different altitudes, with varying power due to the drift in velocity of plasma bubbles. By taking the spectrum of the received signal, we can obtain Doppler frequency and amplitude. From this spectrum, we can extract the drift velocity of the plasma bubbles. Since, many of the plasma phenomena originate in the equatorial region, the location of the radar is quite significant. The frequency of the radar plays an important role as the size of the plasma bubbles and the frequency are related.

II DESIGN PHILOSOPHY

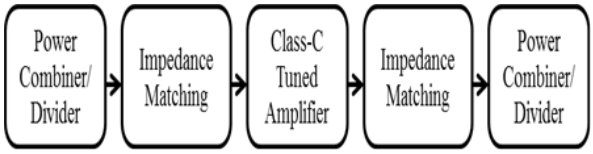

Fig 1: Block diagram of SSPA

Fig 1 shows the basic block diagram of the SSPA. As mentioned earlier, the main part is a Class-C spot frequency tuned power amplifier. The LDMOS transistor used in this design has low input and output impedances; hence impedance matching to 50 Ω is employed on both input and output. As this device has dual LDMOS transistors, a Wilkinson type power splitter is used at the input and power combiner at the output. A lumped element based RF power combiner and divider for the input and output section has been used along with LC impedance matching circuit. The DC power is fed to each of the drain of the LDMOS through Radio Frequency Chokes (RFC) and sufficient decoupling is also provided. Spot frequency tuning is achieved by a parallel LC section connected to the drain in series with RFC.

Power Divider/Combiner (PCD)

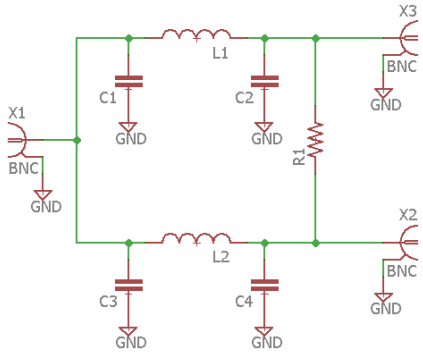

Fig 2: Circuit diagram of Power Divider/Combiner

Fig 2 depicts the Wilkinson type lumped element based power combiner/divider. For a PCD, the impedance of each arm is $\sqrt{N} \times Z$, where N-number of ports and Z-impedance of the port. It has two ports with impedance 50Ω each and contains an impedance of 70.7Ω with phase shift of 90°. The lumped element has π design with a capacitance of 122 pF and inductance of 0.62 µH derived using the following equations $X_C = \frac{1}{2\pi f_C}$ and $X_L = 2\pi f_L$. For calculating the inductance of coil $L_{mH} = \frac{N^2 L}{D^2 A^2}$, from this we get 17 SWG, *13 turns, 12 mm diameter and 37.5mm long* coil.

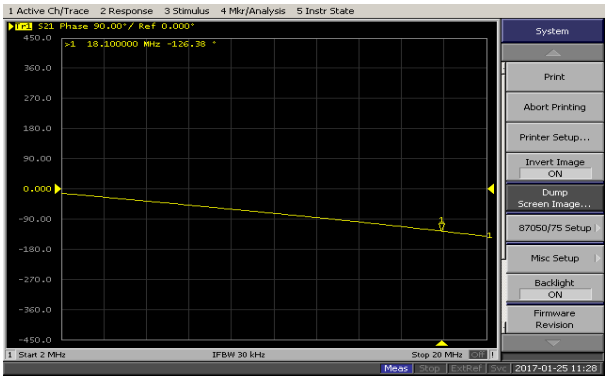

Fig 3a: Phase measurement using VNA

The measured phase shift including the measuring cable having a phase delay of 36° is

shown in fig 3a and impedance is shown in fig 3b respectively. This is used in both input and output sections of the power divider/combiner of the high power RF amplifier.

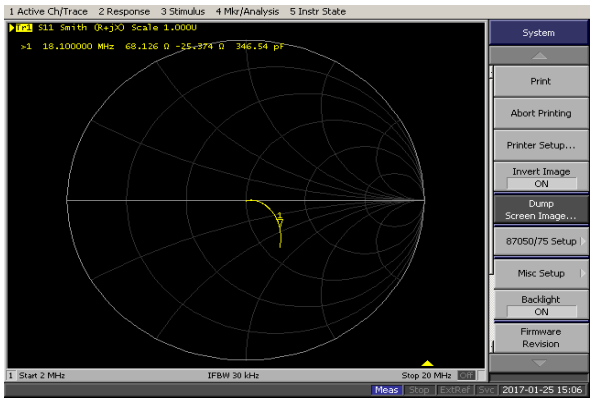

Fig 3b: Impedance measurement from Smith chart using VNA

Impedance Matching Circuits

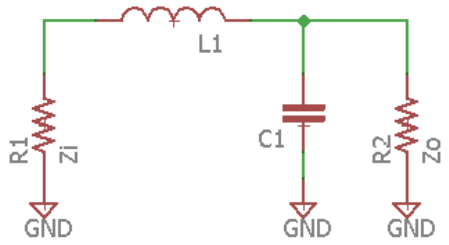

Fig 4: Circuit diagram of input impedance matching

Fig 4 depicts the Circuit diagram of input impedance matching. Mainly impedance matching to 50Ω is required in the circuit owing to the low input and output impedances of the LDMOS transistor. This necessitates the requirement of having compact impedance matching circuits to avoid the power loss. To achieve this, we have designed a tuned LC impedance matching circuit. The input impedance of this transistor is *~2.94-j9.64*, and we need to transfer this impedance to 50Ω. The following equations are used for calculation:

$$Q = Q_S = Q_P = \sqrt{\left(\frac{R_{Larger}}{R_{Smaller}}\right) - 1} \quad \ldots\ldots\ldots (1)$$

$$L_{mH} = \frac{0.159 \times X_L}{f_{GHz}} = \frac{0.159 \times Q_S \times R_{Smaller}}{f_{GHz}} = \frac{0.159 \times R_{Larger}}{f_{GHz} \times Q_P} \quad \ldots\ldots\ldots (2)$$

$$C_{pF} = \frac{159}{f_{GHz} \times X_C} = \frac{159}{f_{GHz} \times Q_S \times R_{Smaller}} = \frac{159 \times Q_P}{f_{GHz} \times R_{Larger}} \quad \ldots\ldots\ldots (3)$$

Where Q is the Quality factor, R_{Larger} is high impedance (50Ω), and $R_{Smaller}$ is low impedance (*2.94-j9.64)*

$$R_{Smaller} = \sqrt{(2.94)^2 + (9.64)^2} = 10.07\Omega$$

Using the above equations, Q can be calculated as follows

$$Q = \sqrt{\left(\frac{50}{10}\right) - 1} = 2$$

Following this, the L_{nH} and C_{pF} has been calculated from equation 2 and 3. The frequency is *18.1MHz*, and therefore, f_{GHz} *=0.0181*. Solving these equations, we get L_{nH}*=175nH and* C_{pF}*=351pF*. But due to the unavailability of these components, we have used closer values i.e, L_{nH}*=165nH (12mm Dia, 4Tuns, 17SWG, Air core)* and $C_{pF=}$ *330pF* respectively. A prototype has been realized and the measured impedance is found to be *54.32Ω (37.65-j39.04) as* shown in Fig 5. This impedance matching has been performed for both the input channels.

The output impedance of the LDMOS transistor is 2.79Ω (*~2.74+j0.57*). In order to convert this impedance to 50Ω an LC circuit is required. To design this matching circuit, the values have been estimated using the same equations mentioned above.

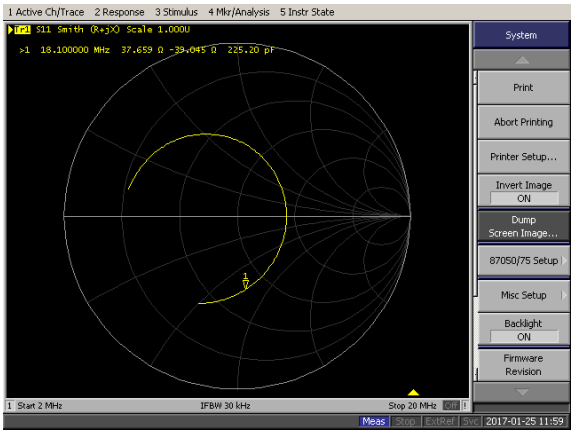

Fig 5: Input Impedance measurement from smith chart using VNA

The estimated values were L_{nH}*=100nH and* $C_{pF=}$ *527pF* and due to the unavailability of the same, closer values .i.e., L_{nH} *=100nH (12mmDia, 3Tuns, 17SWG, Air Core) and* C_{pF} *=470pF* have been used. After incorporating this, the measured impedance value was found to be *56.55 Ω (35.10-j44.34)* and is shown in Fig 6.

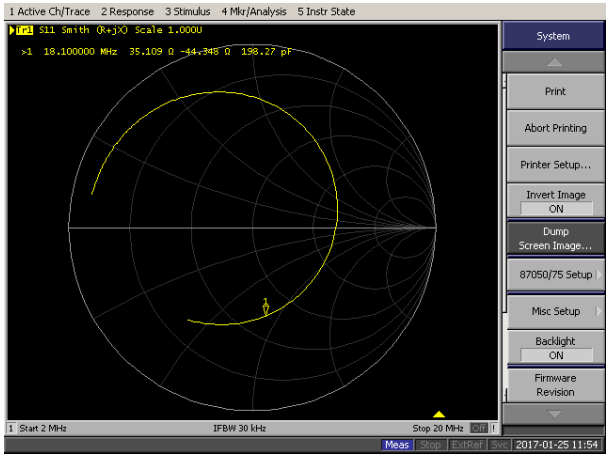

Fig 6: Output Impedance measurement from smith chart using VNA

Class-C Tuned Amplifier

As is known, Class-C tuned amplifiers contain an LC tuned tank circuit in the collector and self-biasing circuit in the base of transistor. Normally for high power Class-C configuration MOS based devices are not preferred. In fact, this is the first attempt to use LDMOS device in high power Class-C mode amplifier. The DC power consumption when RF input is not present is negligible contributing to a better efficiency level.

III DESIGN REALIZATION

The development of SSPA has been initiated with the schematic and RF PCB design which is shown in Fig 7 and Fig 8. The proper grounding, placement of components, positioning of heat sink and heating parts are important in the present PCB. After the design, the PCB has been fabricated using FR-4 material and populated with the components as shown in Fig 9. Soldering in the PCB is done stage by stage along with taking measurements of phase angle, impedance etc. After assembling the full board, it is connected to a test setup with proper RF load as shown in Fig 10. It has been found that the test results were satisfactory and are shown in Fig. 11. The measured parameters are tabulated in Table 1. The endurance test for continuous 48 hours was carried out and found that heat dissipation was negligible along with consistent performance.

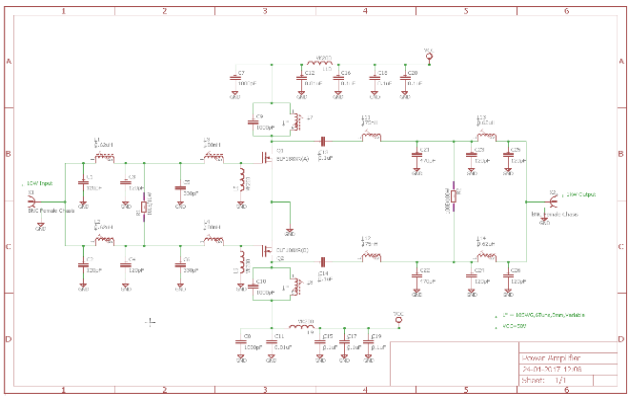

Fig 7: Full Schematic of SSPA

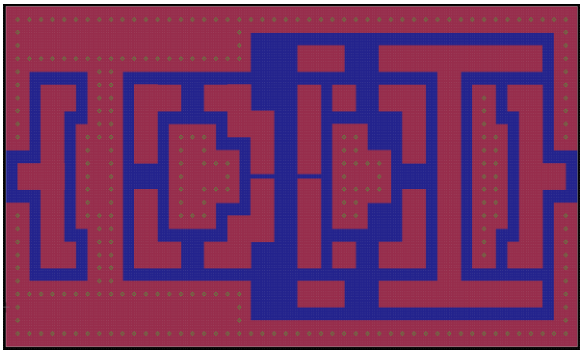

Fig 8: RF PCB Layout of SSPA

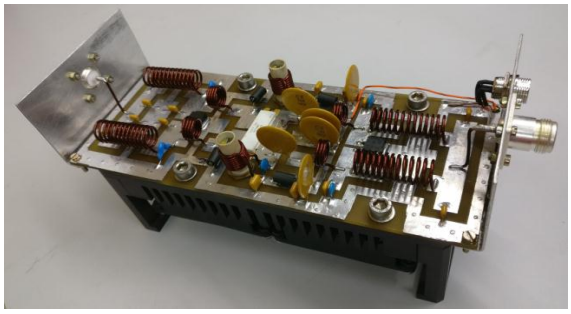

Fig 9: Populated view of SSPA

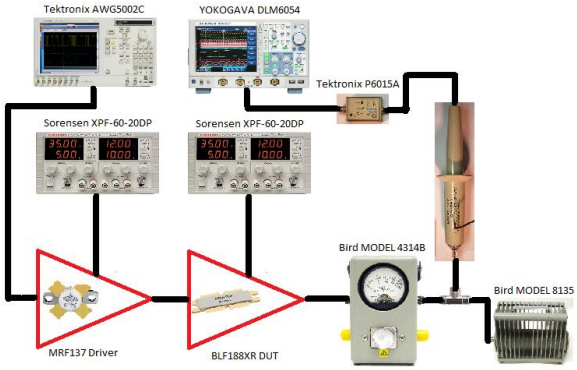

Fig 10: Test setup of SSPA

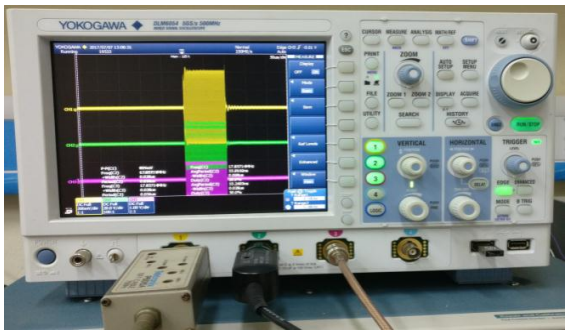

Fig 11: Measured result of SSPA

Channel	i/p V_{pp}	o/p V_{pp}	Pout (W)	Gain (dB)
1	35	660	1089	25.5
2	35	630	992	25.1
Total	50	900	2025	25.1

Table 1: Measured parameters

IV CONCLUSION

Using a single LDMOS transistor, a SSPA module for HF RADAR has been developed, which is located at Thumba Equatorial Rocket Launching Station Trivandrum, Kerala. The design, fabrication, integration and testing have been done at Space Physics Laboratory of VSSC, Trivandrum.

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