

Scalable, Layered, Memory Protected & Fault-tolerance software architecture for Multi-Channel, Multi-Mode Radar Signal Processor for Active Array Radar using Multi Core Processor Hardware

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Abstract:

The major advantage of Active Array Radar is its fault-tolerance capability i.e. the radar can still be operational with degraded performance even if some of the Transmit-Receive modules (TRM) fail in the system. Radar Signal Processor which receives digitized data from the data acquisition system and processes the data for various air-to-air, air-to-sea and air-to-ground mode of operation should not introduce single point failure in the system. The Radar signal processor, without fault-tolerance capability can make advantage of active array inattentive. The Radar Signal Processor for such requirement should have architecture which is scalable, layered, memory protected and fault-tolerant. This paper discusses about one such possible architecture.

Key Words: Radar Signal Processor, Dwells, Beam, Layered, Software, Memory protection, Fault Tolerant Architecture

I INTRODUCTION

Active Array Radar is multi-mode, pulse Doppler radar, operating with low, medium and high PRF waveforms. Radar Signal Processor (RSP) is one of the main sub-systems of the Radar, its purpose is to collect multiple channels of digitized I and Q data from data acquisition system (DAS), and process the data to declare the detected targets. The processed information from RSP is sent to Radar Video Processor (RVP).

The major advantage of Active Array radar is its fault-tolerance capability i.e. the radar can still be operational with degraded performance even if some of the Transmit-Receive modules (TRM) fail in the system [1]. Radar Signal Processor which is the main processing subsystem of radar should not introduce single point failure in the system. The RSP, not having fault-tolerance capability can make advantage of active array inattentive.

The signal processor is a processing intensive subsystem which provides number crunching capability to

the radar; it has very stringent throughput and latency requirements, hence these requirements mandate the use of multiprocessing hardware for radar signal processor.

Signal processor for active array needs to process the data for each radar beam, having different waveforms and timings as per radar's mode of operation; in addition to that each radar beam will have multiple channels to be processed within required time-deadline. The radar signal processor to cater these complex requirements must be fault-tolerant, scalable and reconfigurable for dynamic mode switching. The proposed architecture leads to the realization of Radar Signal Processor on multiprocessor hardware which is scalable, layered, memory protected, fault-tolerant and reconfigurable as it will be discussed in subsequent sections of this paper.

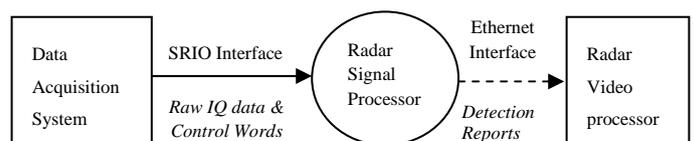


Figure 1: Radar Signal Processor's Context Diagram

II SOFTWARE ARCHITECTURE FOR MULTIPROCESSOR HARDWARE

The radar signal processing is highly compute intensive, hence its implementation mandates the use of multiprocessing hardware which consists of multiple processors / cores interconnected by switch fabric.

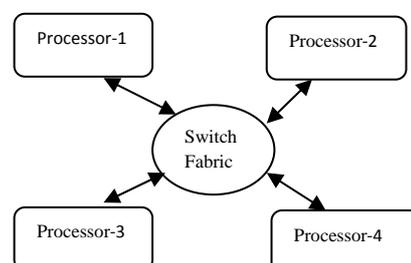


Figure 2: Multiple processors interconnected by switch fabric

RSP needs to process continuous dwells received from data acquisition system, each dwell is an atomic entity which is independent of other dwells, this leads to dynamically scheduling each beam/dwell request to different processor, so that if any of the processor fails in the system, the radar processor will still work with less number of beam request processed.

This leads to decomposition of signal processor software into the multiple S/W modules [2], implemented as multiple Real Time Processes (RTPs) running on different processors [3], these RTPs can be broadly classified into two categories.

- a. Control Element (CE)
- b. Processing Elements (PEs)

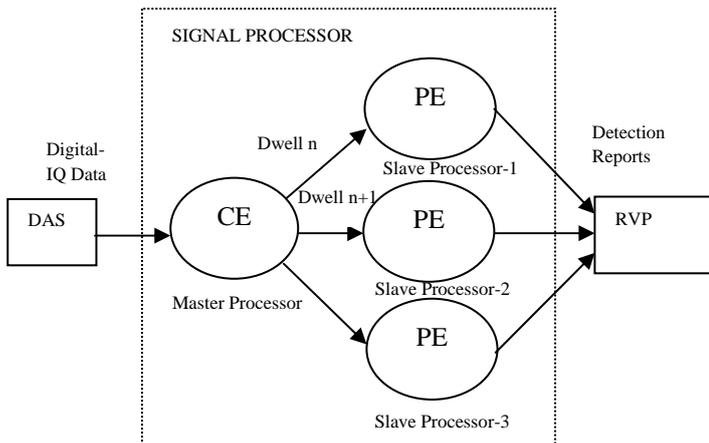


Figure 3: Decomposition of Signal Processor into multiple Processes running on different processors

Control Element RTP runs on the master processor which receives the digital data to be processed from DAS in the form of continuous dwells and dynamically schedules each dwell to a Slave Processor which is free for processing this dwell.

S No	Task	Summary of Operation	Task Implemented in which Layer
1	"Data_Reception"	Data Reception from Digital Interface Card	Hardware Interface Layer
2	"Slave_Status_Get"	Monitor Slave Processors Status if Busy or Available	Data Distribution Layer
3	"Distubute_to_Slave"	Dynamic dwell scheduling to Slave Processors	

Figure 4: Functionalities of control element (CE)

In summary the Control Element is responsible for data reception from DAS and scheduling the processing of dwells amongst other available Slave Processors.

The Processing Element RTPs runs on slave processors, they receive the dwell to be processed from master processor (CE) in the form of set of bursts. Once a full dwell is available for processing, then PE decodes the received control words and invokes the required processing Function based on current mode type field in Control Words and sends the processed reports to RVP.

S No	Task	Summary of Operation	Task Implemented in which Layer
1	"Data_Reception"	Dwell data Reception from Master Processor	Hardware Interface Layer
2	"Invoke_Processing_Mode"	Invokes Appropriate Processing Capability based on Current Mode Type	Switching Layer
3	"SP_Mode-1"	Processing Capability for Mode-1	Signal Processing Layer
4	"SP_Mode-2"	Processing Capability for Mode-2	
5	"SP_Mode-n"	Processing Capability for Mode-n	

Figure 5: Functionalities of processing elements (PEs)

In summary, PEs provides the basic processing capabilities to Signal Processor based on mode of operation.

III LAYERED NATURE OF SOFTWARE ARCHETECTURE

Scalability feature brings advantage of increasing number of processors in a system with minimum modification in the signal processor software design. The proposed software architecture is divided into three layers; those are Hardware Interface Layer, Data Distribution Layer, Switching Layer and Signal Processing layer. The layered architecture offers advantage of isolating processing application from the data reception and data distribution activity, this will be useful when an application needs to be ported to different hardware, keeping application layer same and upgrading the hardware interface and data distribution layer to support new hardware. Adding a new processing mode in a layered architecture can be easily achieved by adding new processing capability in Signal Processing Layer while keeping other layers intact. Each layer can be implemented with separate software tasks or functions.

Active Array Radar needs to process the data for each radar beam, having different waveforms and timings as per radar's mode of operation; in addition to that each radar beam will have multiple channels to be processed. The proposed layered architecture also takes care of such processing requirement effectively.

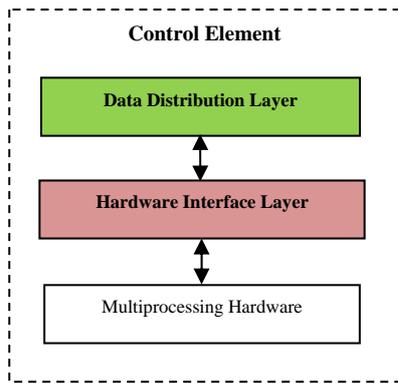


Figure 6: Layered architecture of control element

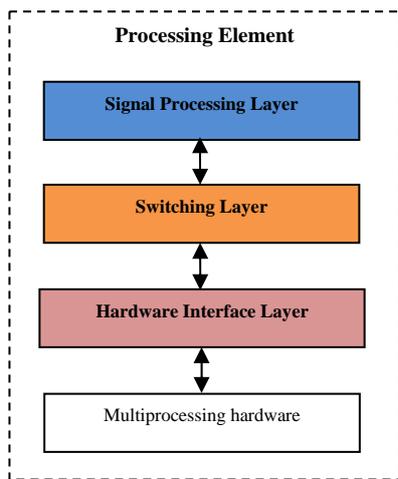


Figure 7: Layered architecture of processing element

Hardware Interface Layer

Hardware Interface Layer is responsible for all data transaction activities over I/O interfaces of processors such as serial RapidIO, Gigabit Ethernet etc; it is the lower most layers hence it is highly dependent on hardware.

In case of Control Element it receives the dwell data from external sub system as DAS, and in case of Processing Element it receives the data from Data Distribution Layer running in Control Element.

Data Distribution Layer

Data Distribution Layer provides its functionality for Master Processor (CE); it is responsible for dynamically scheduling the radar dwells amongst the available Slave Processors (PEs).

There is one task running in this layer which continuously monitors each slave processor status; on receiving any new beam to be processed, this task will identify the processor which is free for performing the required processing, then the data will be transferred to that processor for processing. As this layer does the distribution of dwells to other slave processors over switched fabric, it is dependent on hardware.

Switching layer

This layer is the interface between data reception layer and signal processing layer. Switching layer provides its functionality for Slave Processors (Processing Elements); it works as switch between Data Reception and Signal Processing Layer.

This layer decides the processing algorithms to be applied on the data and based on this decision; appropriate algorithm from the Signal Processing layer is activated. For example, if this layer identifies that air-to-air processing is to be done on the current data then air-to-air processing algorithm is activated from the signal processing layer.

Signal Processing layer

The Signal Processing layer provides its functionalities for slave processors; it provides all the processing capabilities to Signal Processor for required modes of operation.

IV MEMORY PROTECTED ARCHITECTURE

RSP software's sub modules such as Control Element and Processing Elements are implemented as separate real time processes (RTPs), where RTPs are isolated in memory access i.e. each RTP's memory is protected from other RTP's memory as well as from kernel's memory[3], This feature is highly desirable in any airborne radar software.

V CONCLUSION

The proposed architecture leads to the realization of Radar Signal Processor on multiprocessor hardware which is Scalable, Layered, Memory Protected, Fault-tolerant, Portable and Reconfigurable.

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